ADM-PCIE-9V7
User Manual

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	Head Office	US Office
Address:	Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK	10822 West Toller Drive, Suite 250 Littleton, CO 80127
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 - toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

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1 Introduction

The ADM-PCIE-9V7 is a high-performance reconfigurable computing card intended for Data Center applications, featuring Xilinx Virtex UltraScale+ FPGA with four banks of 72-bit DDR4-SDRAM, one QSFP-DD cage, and four FireFly sites.

Figure 1 : ADM-PCIE-9V7 Top View

1.1 Key Features

Key Features

- PCIe Gen3 x16 capable
- 1-slot passive heat sink
- 3/4 length, full profile, x16 edge PCIe form factor
- Four separate banks of 64 bit + ECC (72 bit total) DDR4-2666 SDRAM
- One front panel QSFP-DD cage for a total of 8 channels each capable of 28 Gbps operation (total 224 Gbps)
- Four internal FireFly sites for a total of 16 channels each capable of 28Gbps operation (total 448 Gbps)
- Supports VU9P and VU13P Virtex UltraScale+ FPGAs in the D2104 package
- Front panel and rear edge JTAG access via USB port
- FPGA configurable over USB/JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- 8 GPIO signals and 1 isolated timing input
- 4 user LEDs

1.2 Order Code

See the 9V7 datasheet for complete ordering options.

2 Board Information

2.1 Physical Specifications

The ADM-PCIE-9V7 complies with PCI Express CEM revision 4.0.

Description	Measure
PCB Dy	111.15 mm
PCB Dx	254 mm
PCB Dz	1.6 mm
PCB Weight (with components)	200 grams

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	126 mm
Total Dx	352.0 mm
Total Dz	19.0 mm
Total Weight	821 grams

Table 2 : 1-Slot Mechanical Dimensions (Fully Assembled)

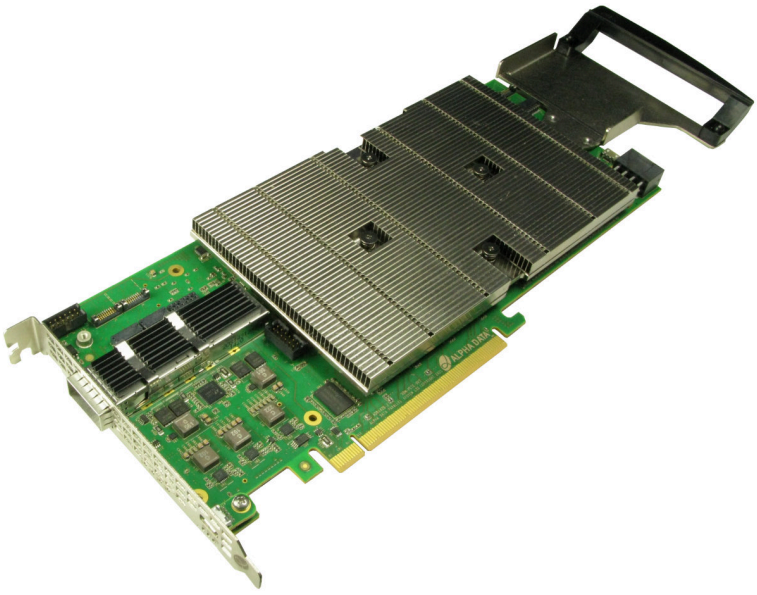

Figure 2 : ADM-PCIE-9V7 1-slot Product Photo

Description	Measure
Total Dy	126 mm
Total Dx	352.0 mm
Total Dz	39.3 mm
Total Weight	865 grams

Table 3 : 2-Slot Mechanical Dimensions (Fully Assembled)

Figure 3 : ADM-PCIE-9V7 2-slot Product Photo

The rear handle is easily installed or removed with three Philips screws accessible on the bottom side of the PCB.

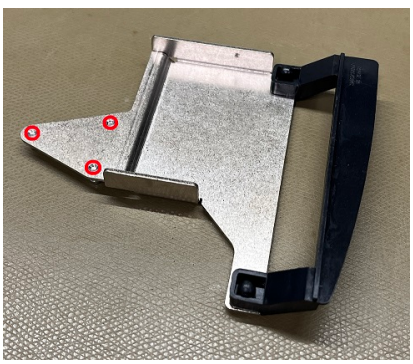

Figure 4 : Full length handle

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-9V7 is capable of PCIe Gen 1/2/3 with 1/4/8/16 lanes, when using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

A 16 lane physical PCIe slot is required for mechanical compatibility.

It is possible to operate this product standalone with power from the 8-pin ATX power connector alone. This requires a small build change to the board. Please contact **sales@alpha-data.com** for details.

The card is also designed to use the extra mechanical retention mechanisms defined in the PCIe specification. This includes both the board keep out region along the top edge, and the full-length handle support. It is recommended to use all board retention features supported by the host systems. These cards are heavy and can be damaged when used in systems that do not mechanically support the hardware properly.

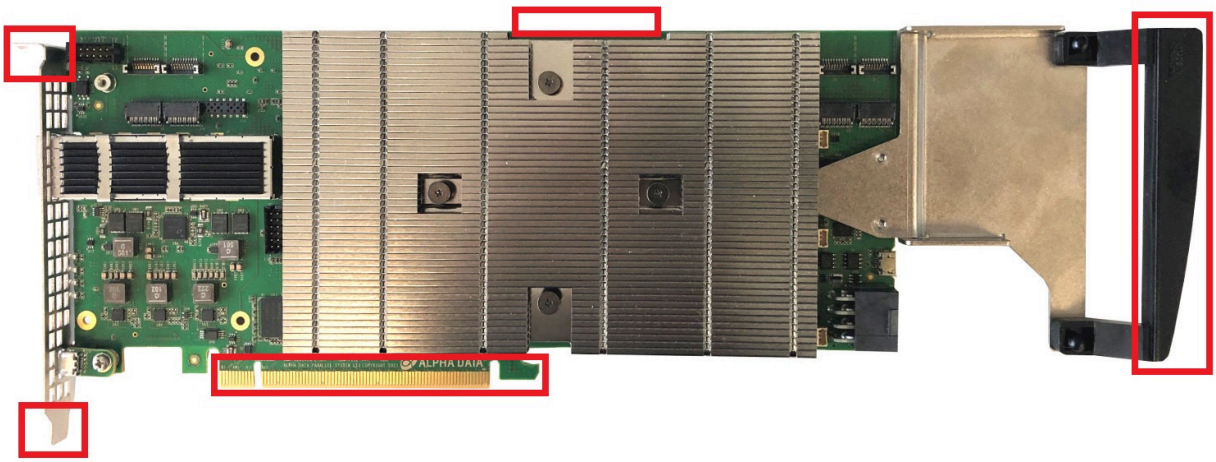

Figure 5 : Retention Points

2.2.3 Power Requirements

The ADM-PCIE-9V7 draws power from the PCIe Edge and the 8-pin ATX power connector. The ADM-PCIE-9V7 does not use or require the 3.3V power from the PCIe Edge (though it does use 3.3V AUX). To operate with PCIe edge only, ensure SW1-7 is OFF (see Switches). As per PCIe specification, users should limit the board power consumption to 66W when using only the PCIe edge power. Adding the 8-pin ATX connector provides additional 108W of power, bringing the total board power dissipation maximum to 174W.

It is possible to operate this product standalone with power from the 8-pin ATX power connector alone. Please be aware this reduces the total rated power of the card to 150W. Standalone operation requires a modified ATX power cable where the sense wires have been removed. Please contact **sales@alpha-data.com** to receive a modified ATX extension cable. When using a cable with the sense wires removed, ensure SW1-7 is set OFF which enables the 12V auto-detect feature. If SW1-7 is ON, the board will not power up unless both PCIe edge and the Aux cable are both used.

Power consumption estimation requires the use of the Xilinx XPE spreadsheet (www.xilinx.com/products/technology/power/xpe.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85-0.90	VCC_INT + VCCINT_IO + VCC_BRAM	120A
0.9	MGTAVCC	6A
1.2	MGTAVTT	12A
1.2	VCCO	10A
1.8	VCCAUX + VCCAUX_IO + VCCO_1.8V	6A
1.8	MGTVCCAUX	1A
3.3	3.3V for Optics	5A

Table 4 : Available Power By Rail

2.3 Thermal Performance

If the FPGA core temperature exceeds 105 degrees Celsius, the FPGA design will be cleared to prevent the card from over-heating.

The ADM-PCIE-9V7 comes with a heat sink to avoid thermal overstress of FPGA, since it is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius. To estimate the FPGA die temperature: first take your total board power (see next paragraph), then multiply by Theta JA from the table below, and add the resulting temperature to your system internal ambient temperature.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the Xilinx Power Estimator (XPE) downloadable at www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the device according to your part number details: Virtex UltraScale+, VU13P/VU9P, D2104 package, -2/-3 speed grade, extended. Set the ambient temperature to your system ambient and select 'user override' for the effective theta JA. Then enter the figure associated with your system LFM in the blank field. When using our 2-slot option with integrated fans use 0.32degC/W. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the 9V7 power estimator from Alpha Data by contacting **support@alpha-data.com**. Enter in the power figures from XPE, optical modules (if used), and DRAM utilization into the Alpha Data spreadsheet to get a complete board level estimate.

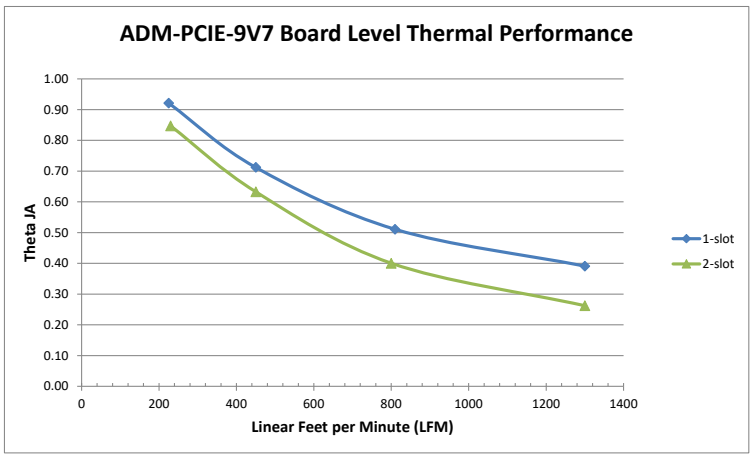

Figure 6 : Thermal Performance

The 2-slot option for the ADM-PCIE-9V7 offer a significant advantage from a thermal effeciency standpoint. The integrated blowers can be easily removed by removing the two screws in the stiffening bracket as shown below:

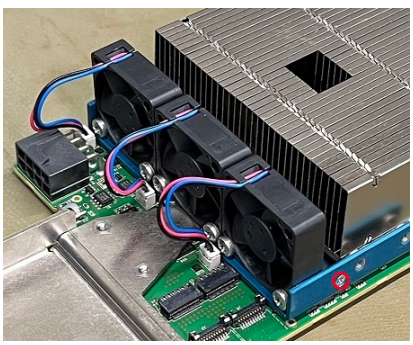

Figure 7 : Integrated Fans

2.4 Customizations

Alpha Data provides extensive customization options to existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: additional networking cages in adjacent slots, enhanced heat sinks, baffles, and circuit additions.

Please contact **sales@alpha-data.com** to get a quote and start your project today.

3 Functional Description

3.1 Overview

The ADM-PCIE-9V7 is a versatile reconfigurable computing platform with a Virtex UltraScale+ VU9P/VU13P FPGA, a Gen3x16 PCIe interface, four banks of DDR4-2666 each 72 bits wide (for 64 bits with 8 bits ECC), one QSFP-DD cage capable of 8x 28G with any Xilinx supported standard (Ethernet, SRIO, InfiniBand, etc.), four Samtec FireFly sites also capable of 28G/channel in either optical or copper cabling, a 12 pin header for general purpose use (clocking, control pins, debug, etc.), and a robust system monitor.

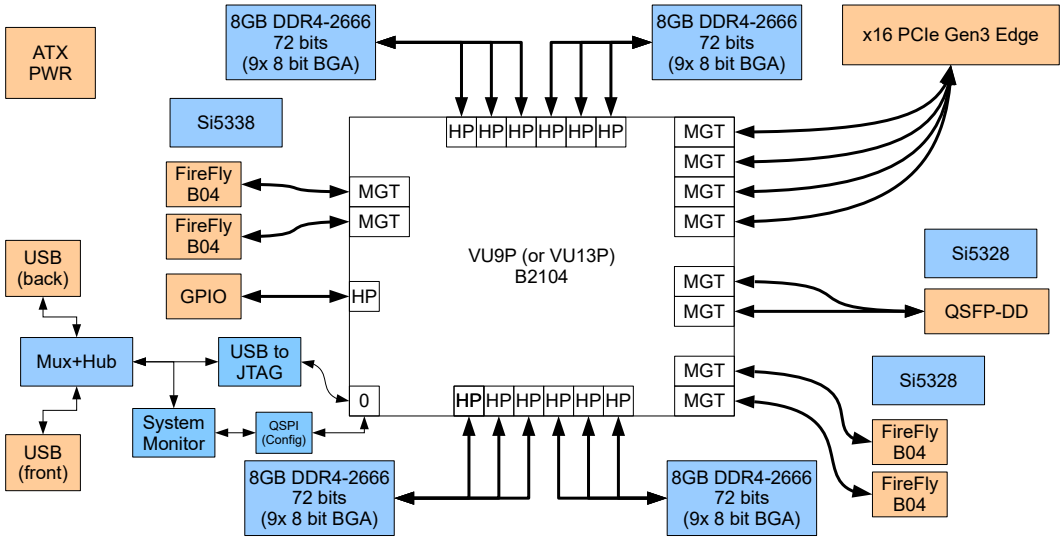

Figure 8 : ADM-PCIE-9V7 Block Diagram

3.1.1 Switches

The ADM-PCIE-9V7 has an octal DIP switch SW1, located on the rear side of the board. The function of each switch in SW1 is detailed below:

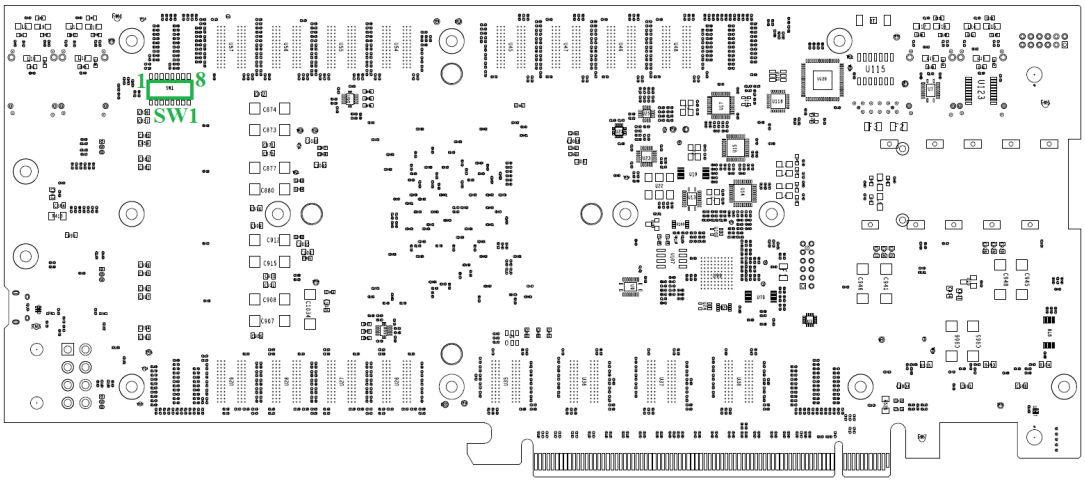

Figure 9 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch 0	Pin D21 = '1'	Pin D21 = '0'
SW1-2	OFF	User Switch 1	Pin D18 = '1'	Pin D18 = '0'
SW1-3	OFF	Reserved	TBD	TBD
SW1-4	OFF	Reserved	TBD	TBD
SW1-5	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW1-6	OFF	HOST_I2C_EN	System Monitor connected to PCIe slot I2C	System Monitor isolated from PCIe slot I2C
SW1-7	ON	12V Auto-detect	12V auto-detect enabled	8-pin ATX cable and PCIe edge both required
SW1-8	OFF	Power Off	Board will power up	Immediately power down

Table 5 : Switch Functions

Use I/O Standard "LVCMOS18" when constraining the User Switch pins.

3.1.2 LEDs

There are 7 LEDs on the ADM-PCIE-9V7, 4 of which are general purpose and whose meaning can be defined by the user. The other 3 have fixed functions described below:

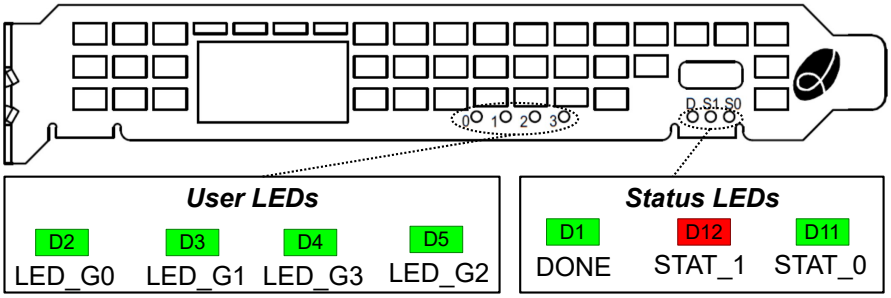

Figure 10 : Front Panel LEDs

Comp. Ref.	Function/Net Name	ON State	OFF State
D2	USER_LED_0_1V8	User defined '0'	User defined '1'
D3	USER_LED_1_1V8	User defined '0'	User defined '1'
D4	USER_LED_2_1V8	User defined '0'	User defined '1'
D5	USER_LED_3_1V8	User defined '0'	User defined '1'
D1	DONE	FPGA is configured	FPGA is not configured
D12	Status 1	See Status LED Definitions	
D11	Status 0	See Status LED Definitions	

Table 6 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 Clocking

The ADM-PCIE-9V7 provides flexible reference clock solutions for the many multi-gigabit transceiver quads, DDR4 banks, and FPGA fabric. Any programmable clock, from the Si5338 Clock Synthesizer, is reconfigurable from the front panel USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency is 350MHz. Customers who purchase RD-9V7 also have the option of embedding IP into their FPGA design that permits programmable clock reconfiguration via PCIe or from within the FPGA.

There are three available Si5328 jitter attenuator. These can provide clean and synchronous clocks to the QSFP-DD and Samtec FireFly quad locations at many clock frequencies. These devices use volatile memory, so the FPGA design will need to reconfigure the register map over I2C after any power cycle or FPGA reconfiguration event.

All clock names in the section below can be found in Complete Pinout Table.

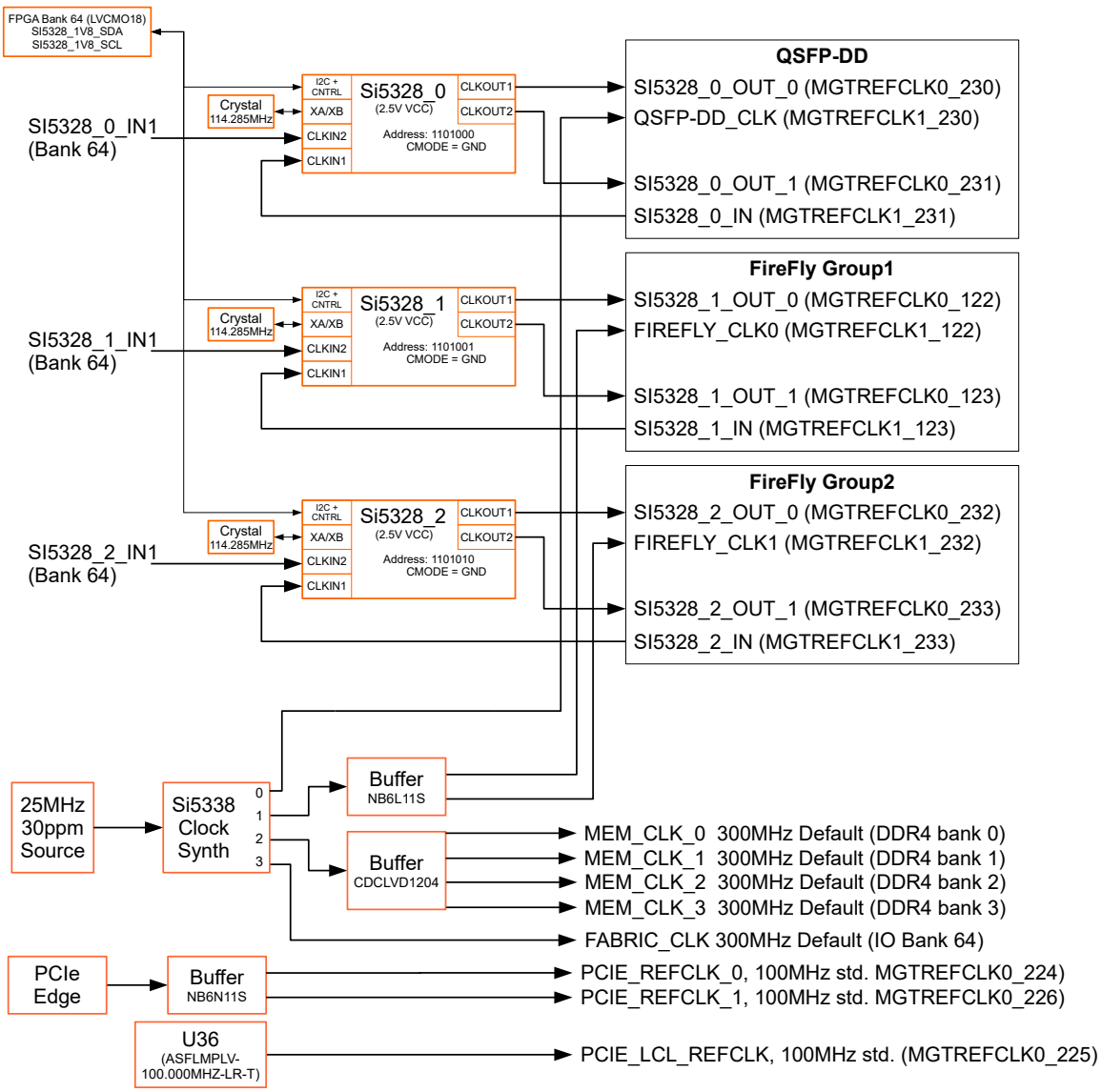

Figure 11 : Clock Topology

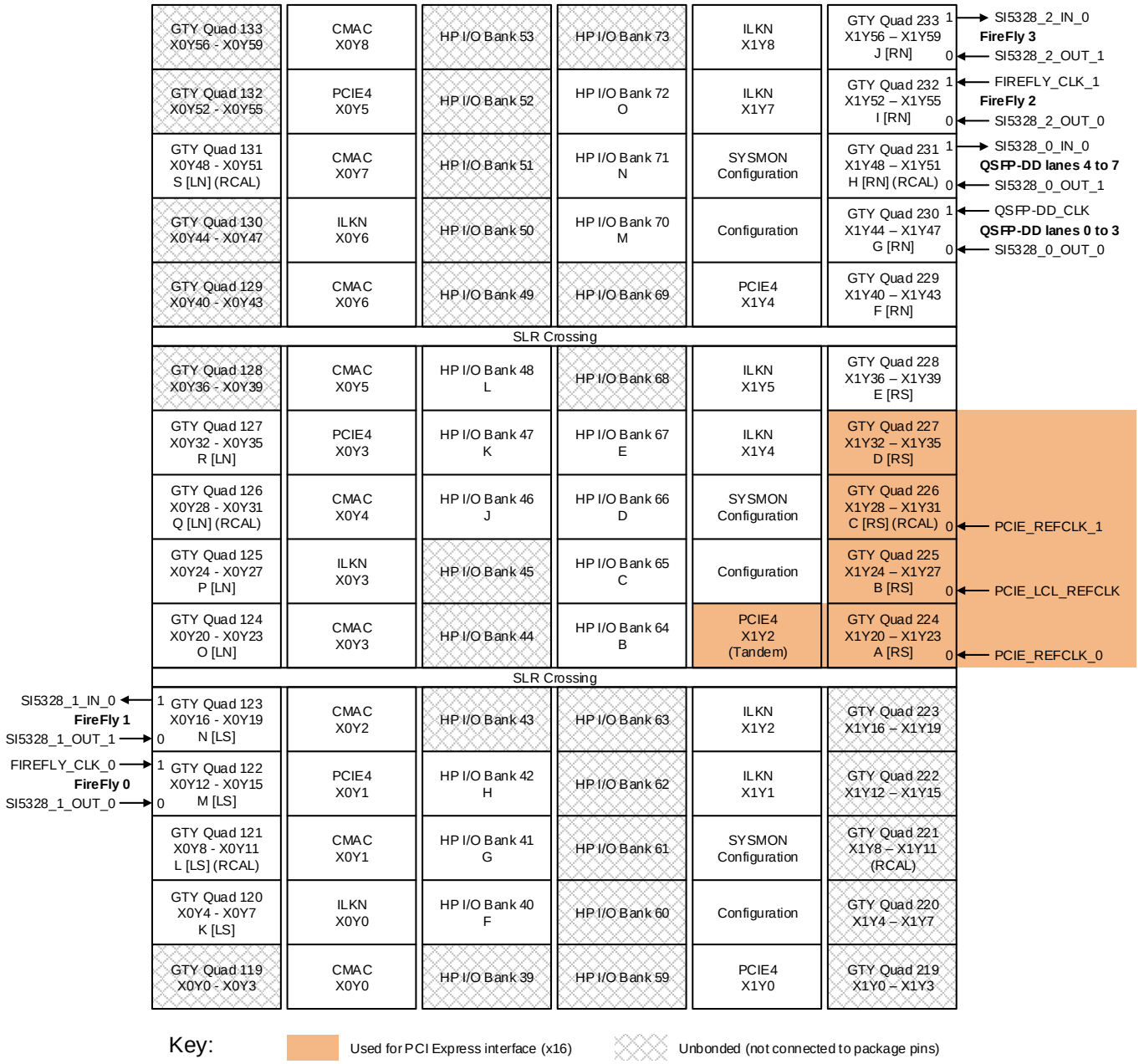

Figure 12 : VU9P FPGA Clock Location

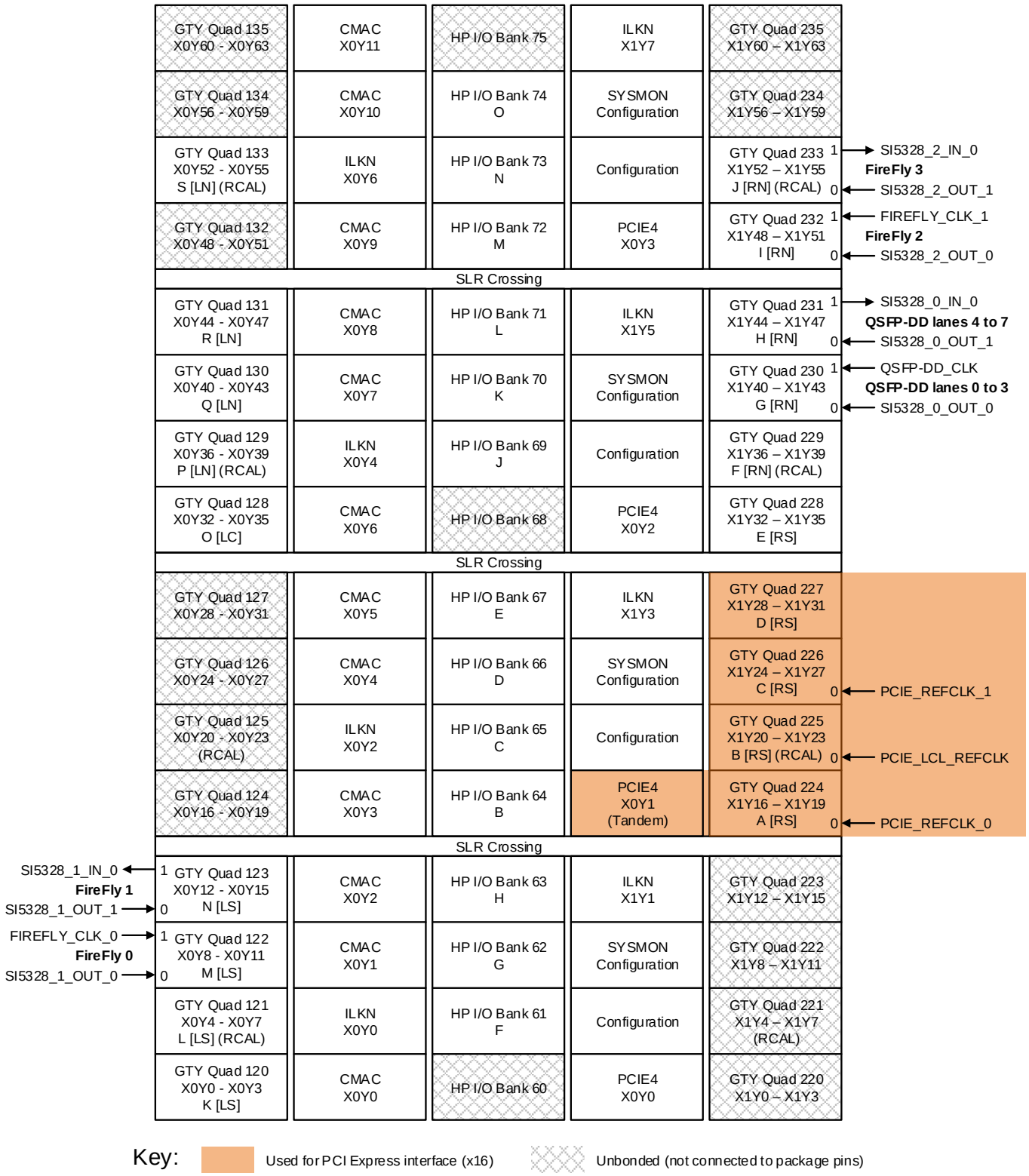

Figure 13 : VU13P FPGA Clock Location

3.2.1 Si5328

If jitter attenuation is required please see the reference documentation for the Si5328.
www.silabs.com/Support%20Documents/TechnicalDocs/Si5328.pdf

There are two input clock options. Si5328 pin CLKIN1 (board net name SI5328_*_IN_0_P/N) of each Si5328 is connected to an MGT clock output for the most direct clock recovery architecture. Si5328 pin CLKIN2 (board net name SI5328_*_IN_1_P/N) of each Si5328 is connected to a clock capable GPIO pin similar to the Xilinx VCU108 Development Kits (page 57 of the schematic, component U57). The MGT RXOUTCLK can be used to pass a recovered clock to the FPGA fabric. Please refer to Xilinx UG578 and the VCU108 for more information.

The INT_C1B and LOL signals for each component are available for use, and can be located at net names SI5328_*_1V8_INT_C1B and SI5328_*_1V8_LOL in the Complete Pinout Table.

The active low reset of each Si5328 is accessible to the FPGA. See net names SI5328_*_1V8_RST_L in the Complete Pinout Table.

> **Note:**
> Each active low reset has an external pull-down resistor, which will reset the Si5328 when unused to save power. This pin must be actively driven high to maintain the programmed register map and running clocks.

The Si5328 configuration register map is volatile, and must be written on each power up event over I2C. Use nets SI5328_1V8_SDA and SI5328_1V8_SCL at pins located in the Complete Pinout Table. The three Si5328 devices onboard are each strapped to a different I2C address register as detailed in the table below.

Index	7bit Hex Address	Binary Address
Si5328_0	68	110_1000
Si5328_1	69	110_1001
Si5328_2	6A	110_1010

Table 7 : Si5328 address table

3.2.2 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT tiles 224 through 227 and use the host system's 100 MHz PCIe reference clock (net name PCIE_REFCLK_0_P/N or PCIE_REFCLK_1_P/N in the Complete Pinout Table).

Alternatively, a more stable but asynchronous onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK_P/N in the Complete Pinout Table).

3.2.3 Fabric Clock

The design offers a fabric clock (net name FABRIC_CLK_P/N) which defaults to 300 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

Use constraints DIFF_TERM_ADV = TERM_100 and IOSTANDARD LVDS for this reference clock.

See net names FABRIC_CLK_P/N in the Complete Pinout Table for pin locations.

3.2.4 Programming Clock (EMCCLK)

A 125MHz clock (net name EMCCLK_PIN in the Complete Pinout Table) is fed into the EMCCLK pin to drive the SPI flash device during configuration of the FPGA. Note that this is not a global clock capable IO pin and runs at a fixed frequency.

3.2.5 QSFP-DD Clock

The QSFP-DD clock has a default 156.25MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

See net names QSFP-DD_CLK_P/N in the Complete Pinout Table for pin locations.

The QSFP-DD cage is also configured such that it can be clocked from an Si5328 jitter attenuator.

Pin locations of net names SI5328_0_OUT_*_P/N can be located in the Complete Pinout Table.

3.2.6 Samtec FireFly Clock

The FireFly clocks have a default 156.25MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

See net names FIREFLY_CLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

The FireFly quads are also configured such that it can be clocked from an Si5328 jitter attenuator.

See net names SI5328_1_OUT_*_P/N and SI5328_2_OUT_*_P/N in the Complete Pinout Table for pin locations.

3.2.7 Memory Clocks

Each of the four memory banks has their own buffered 300MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 350MHz by re-programing the Si5338 reprogrammable clock oscillator. See details on avr2util in the section: USB Interface.

See net names MEM_CLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

See DDR4 SDRAM for mor information on the memory banks and their physical locations.

These clocks should be constrained as DIFF_SSTL_12. Differential termination, DC bias, and level shifting are provided external to the FPGA.

3.3 PCI Express

The ADM-PCIE-9V7 is capable of PCIe Gen 1/2/3 with 1/4/8/16 lanes and PCIe Gen 4 with 1/4/8 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) is connected to the FPGA through a buffer. See Complete Pinout Table signal PERSTN0.

The pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table, see net names PCIE_TX*_PIN_P/N and PCIE_RX*_P/N.

The PCI Express specification requires that all add-in cards be ready for enumeration within 120ms after system power is valid (100ms after power is valid + 20ms after PERST is released). The ADM-PCIE-9V7 does meet this requirement when configured from a tandem bitstream with the proper SPI constraints detailed in the Configuration From Flash Memory section. For more details on tandem configuration, see Xilinx xapp 1179.

3.4 DDR4 SDRAM

Four banks of DDR4 SDRAM memory are soldered down to the board. The available density of the memory is 8GB/per bank, 32GB total. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 2666 MT/s.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. An example memory exerciser project is included in the RD-9V7. All pin location information is included in Complete Pinout Table.

> **Note:**
> DDR4 bank 1 cannot be used with the Xilinx tandem programming flow.

The 8Gb components used are Micron MT40A1G8SA-075:E

Simulation results show that the address command bus has additional margin when constrained with medium slew strength and 60 ohm drivers. For example, net A0 of bank 0 could be constrained with these xdc commands:

```
set_property SLEW MEDIUM [ get_ports "c0_ddr4_adr[0]" ]

set_property OUTPUT_IMPEDANCE RDRV_60_60 [ get_ports "c0_ddr4_adr[0]" ]
```

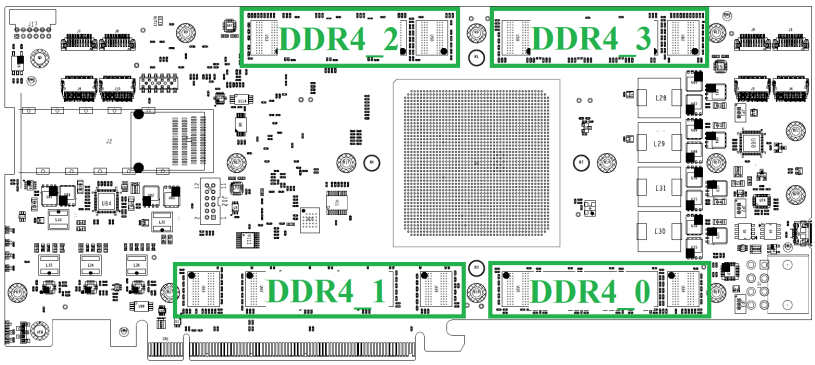

Figure 14 : DDR4 bank locations by index

3.5 QSFP-DD

One QSFP-DD cage is available at the front panel. This cage is capable of housing either QSFP28 or QSFP-DD cables (QSFP-DD is backwards compatible with QSFP). Both active optical and passive copper QSFP-DD/ QSFP28 compatible models are fully compliant. The communication interface can run at up to 28Gbps per channel. The QSFP-DD cage has 8 channels (total maximum bandwidth of 224Gbps per cage). This cage is ideally suited for 8x 10G/25G, 2x 100G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All QSFP-DD cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is QSFP_*, with locations clarified in the diagram below.

The management interface of the QSFP-DD cage is connected directly to the FPGA as detailed in Complete Pinout Table.

QSFP-DD spec. name	Board net name	External resistor
SCL	QSFP_SCL_1V8	Pull-up
SDA	QSFP_SDA_1V8	Pull-up
IntL	QSFP_INT_1V2_L	Pull-up
ResetL	QSFP_RST_1V8_L	Pull-up
ModSelL	N/A	Hard GND
ModPrsL	QSFP_MODPRS_1V2_L	Pull-up
LPMode	QSFP_LPMODE_1V8	Pull-down

Table 8 : QSFP-DD management interface

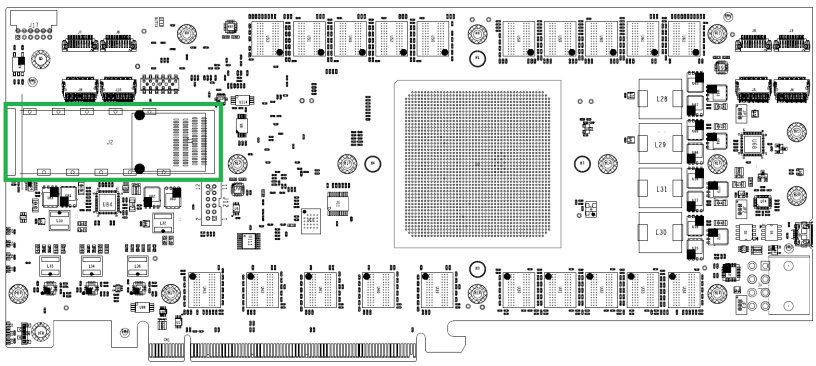

Figure 15 : QSFP-DD Location

It is possible for Alpha Data to pre-fit the ADM-PCIE-9V7 with QSFP-DD and QSFP28 components. Please contact **sales@alpha-data.com** for full details and options.

Alpha Data has tested an array of passive cables from multiple manufacturers. Please contact **sales@alpha-data.com** for more details on appropriate and available cables. Cable types include: QSFP-DD to 8x SFP, QSFP-DD to 2x QSFP, and QSFP-DD to QSFP-DD.

For the latest QSFP-DD specification, please visit www.qsfp-dd.com/specification/

3.6 FireFly

4 FireFly sites are available on the circuit board. All sites are capable of hosting either active optical or passive copper FireFly connectors. The communication interface can run at up to 28Gbps per channel in either cable type. There are 16 channels between the 4 FireFly sites (total maximum bandwidth of 448Gbps). These cages are ideally suited for 16x 10G/25G, 4x 100G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

All FireFly sites have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is FIREFLY* with locations clarified in the diagram below.

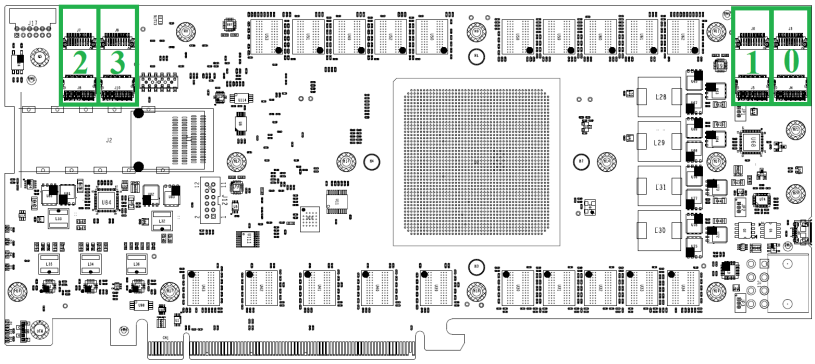

Figure 16 : FireFly Locations

The management interface of each FireFly module is connected directly to the FPGA. To reduce pin count, the SDA, SCL, reset, and interrupt pins are shared. A reset is sent to all modules simultaneously, and an interrupt could originate from any module. To select which module is targeted by the SDA and SCL pins, drive only one MODSEL pin low at a time. See net names in the Complete Pinout Table for pin locations.

FireFly spec. name	Board net name	External resistor
SCL	FIREFLY_SCL_1V8	Pull-up
SDA	FIREFLY_SDA_1V8	Pull-up
IntL	FIREFLY_INT_1V8_L	Pull-up
ResetL	FIREFLY_RST_1V8_L	Pull-up
ModSelL for FireFly0	FIREFLY0_MODSEL_1V8_L	Pull-up
ModSelL for FireFly1	FIREFLY1_MODSEL_1V8_L	Pull-up
ModSelL for FireFly2	FIREFLY2_MODSEL_1V8_L	Pull-up
ModSelL for FireFly3	FIREFLY3_MODSEL_1V8_L	Pull-up
ModPrsL for FireFly0	FIREFLY0_MODPRS_L	Pull-up
ModPrsL for FireFly1	FIREFLY1_MODPRS_L	Pull-up
ModPrsL for FireFly2	FIREFLY2_MODPRS_L	Pull-up
ModPrsL for FireFly3	FIREFLY3_MODPRS_L	Pull-up

Table 9 : FireFly management interface

There is an opening in the 2-slot mechanical design to allow FireFly cables to pass out of the shroud.

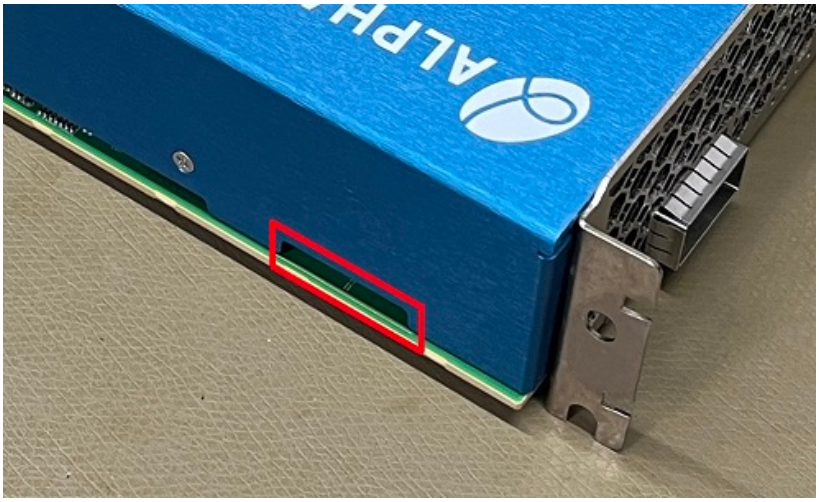

Figure 17 : FireFly Opening

Line rate	Electrical/Optical	9V7 slot configuration	FireFly part number
0-28Gbps	Electrical	1 or 2-slot	ECUE-08-XXX-T3-FF-B4-2-D1
10-14Gbps	Optical	1 or 2-slot	ECUO-B04-14-XXX-0-4-5-01
16Gbps	Optical	1 or 2-slot	ECUO-B04-16-XXX-0-4-5-01
25Gbps	Optical	2-slot only	ECUO-B04-25-XXX-0-5-5-01
28Gbps	Optical	2-slot only	ECUO-B04-28-XXX-0-5-5-01

Table 10 : Recommended FireFly part numbers

Note that "XXX" = overal length in centimeters.
Here is the web link for the optical FireFly detailed prints.
Here is the web link for the optical FireFly catalog page.
Here is the web link for the copper FireFly catalog page.

3.7 System Monitor

The ADM-PCIE-9V7 has the ability to monitor select temperatures, voltages, and currents in order to provide an indication of board health. The monitoring is implemented using an AVR microcontroller. This information can be read out via USB using the avr2util utility. Alternatively, the sensor information can be read directly by the FPGA or via PCIe if RD-9V7 is purchased (reference design package).

If the core FPGA temperature exceeds 105 degrees Celsius, the FPGA image will be cleared to prevent damage to the card.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_AUX	ADC00	12V board input supply from 8-pin ATX Cable
12V_AUX_I	ADC01	12V input current from 8-pin ATX Cable in amps
12V_EDGE	ADC02	12V board input supply from PCIe Edge
12V_EDGE_I	ADC03	12V board input current from PCIe Edge in amps
3V3_AUX	ADC04	3.3V auxiliary board input supply from PCIE edge
3V3_DIG	ADC05	3.3V generated onboard for QSFP optics
2V5_CLK	ADC06	2.5V generated onboard for clock circuitry
2V5_DIG	ADC07	2.5V generated onboard for clock circuitry
1V8_DIG	ADC08	1.8V generated onboard for FPGA IO voltage (VCCO)
0V9_AVCC	ADC09	0.9V generated onboard for transceiver Power (AVCC)
1V2_AVTT	ADC10	1.2V generated onboard for transceiver Power (AVTT)
1V2_DIG	ADC11	1.2V generated onboard for SDRAM and FPGA (VCCO)
1V8_MGT_AUX	ADC12	1.8V generated onboard for transceiver power (AVCC_AUX)
VCC_INT	ADC13	0.85-0.90V generated onboard for VccINT + VccBRAM + VccINT_IO
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature near back edge (U105)
Board1_Temp	TMP02	Board temperature near front panel (U104)
FPGA_Temp	TMP03	FPGA on-die temperature

Table 11 : Voltage, Current, and Temperature Monitors

3.7.1 System Monitor Status LEDs

LEDs D12 (Red) and D11 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 12 : Status LED Definitions

3.8 USB Interface

The FPGA can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PCIE-9V7 utilizes the Digilent USB-JTAG converter which is supported by the Xilinx software tool suite. Simply connect a micro-USB AB type cable between the ADM-PCIE-9V7 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure the FPGA and the SPI configuration Flash memory.

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use this command to see all options:

```
avr2util.exe /?
```

Use this command to display all sensor values:

```
avr2util.exe /usbcom com4 display-sensors
```

Here is an example of changing the FIREFLY_CLK to 100MHz on the next power-up event:

```
avr2util.exe /usbcom com4 setclknv 1 100000000
```

Setclk index 0 = QSFP-DD_CLK, index 1 = FIREFLY_CLK, index 2 = MEM_CLK*, index 3 = FABRIC_CLK.

In the examples above, change 'com4' to match the com port number assigned under windows device manager.

3.9 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-9V7:

- From Flash memory, at power-on, as described in Section 3.9.1
- Using USB cable connected at either USB port Section 3.9.2

3.9.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from a 2 Gbit QSPI flash memory device configured as an x4 SPI device (Micron part numbers MT25QU02GCBB8E12). This flash device is typically divided into two regions of 128 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU9P or VU13P FPGA.

The ADM-PCIE-9V7 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using Windows Device Manager or “lspci” in Linux) in order to provide confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

At power-on, the FPGA attempts to configure itself automatically in SPI master mode, depending on the header of the bitstream that has been flashed into the card. This normally results in SPIx4 configuration at EMCCLK frequency. The configuration scheme used in the ADM-PCIE-9V7 is compatible with Multiboot; see Xilinx UG570 for details. The FPGA can also reconfigure itself from an arbitrary Flash address using the ICAPE3 primitive; this is also described in Xilinx UG570.

The image loaded can support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field update also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.9.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 256
- -interface SPIx4
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)

Program with vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu02g-spi-x1_x2_x4
- State of non-config mem I/O pins: Pull-none

3.9.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908

3.10 GPIO Connector

The GPIO option consists of a versatile shrouded connector from Molex with part number 87832-1222. This connector gives users eight signals connected to the FPGA.

Recommended mating plug: Molex 0875681273 or 0511101260

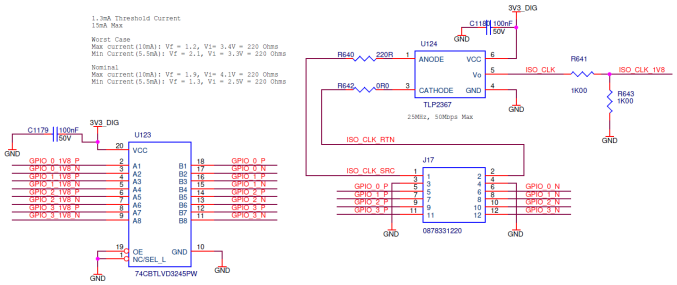

Figure 18 : GPIO Connector Schematic

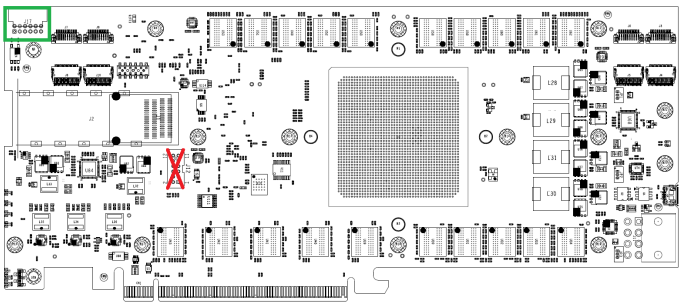

Figure 19 : GPIO Connector Location

3.10.1 Direct Connect FPGA Signals

8 nets are broken out to the GPIO header, as four sets of differential pairs. These signal are suitable for any 1.8V signaling standards supported by the Xilinx UltraScale architecture. See Xilinx UG571 for IO options. LVDS and LVCMOS18 are common options. The 0th and 1st GPIO signal index are suitable for a global clock connection.

The direct connect GPIO signals are limited to 1.8V by a quickswitch (74CBTLVD3245PW) in order to protect the FPGA from overvoltage on IO pins. This quickswitch allows the signals to travel in either direction with only 4 ohms of series impedance and less than 1ns of propagation delay. The nets are directly connected to the FPGA after the quickswitch.

Direct connect signal names are labeled GPIO_*_1V8_P/N to show polarity and grouping. The signal pin allocations can be found in Complete Pinout Table

3.10.2 Timing Input

Pins 1 and 2 of J1 can be used as an isolated timing input signal (up to 25MHz). Applications can either directly connect to the GPIO connector, or Alpha Data can provide a cabled solution with an SMA or similar connector on the front panel. Contact **sales@alpha-data.com** for front panel connector options.

For pin locations, see signal name ISO_CLK in Complete Pinout Table.

The signal is isolated through a optical isolator part number TLP2367 with 220 ohm of series resistance.

3.11 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

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Appendix A: Complete Pinout Table

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
BA19	AVR_B2U_1V8	IO_L18P_T2U_N10_AD2P_64	IO_L18P_T2U_N10_AD2P_64	1.8
BB21	AVR_MON_CLK_1V8	IO_L17P_T2U_N8_AD10P_64	IO_L17P_T2U_N8_AD10P_64	1.8
BB19	AVR_U2B_1V8	IO_L18N_T2U_N11_AD2N_64	IO_L18N_T2U_N11_AD2N_64	1.8
AK13	CCLK	CCLK_0	CCLK_0	1.8
AY28	DDR4_0_A0	IO_L13N_T2L_N1_GC_QBC_40	IO_L13N_T2L_N1_GC_QBC_61	1.2
BB26	DDR4_0_A1	IO_L7P_T1L_N0_QBC_AD13P_40	IO_L7P_T1L_N0_QBC_AD13P_61	1.2
BB29	DDR4_0_A10	IO_L8N_T1L_N3_AD5N_40	IO_L8N_T1L_N3_AD5N_61	1.2
BC26	DDR4_0_A11	IO_L7N_T1L_N1_QBC_AD13N_40	IO_L7N_T1L_N1_QBC_AD13N_61	1.2
AU30	DDR4_0_A12	IO_L16N_T2U_N7_QBC_AD3N_40	IO_L16N_T2U_N7_QBC_AD3N_61	1.2
BE26	DDR4_0_A13	IO_L1N_T0L_N1_DBC_40	IO_L1N_T0L_N1_DBC_61	1.2
AW29	DDR4_0_A14	IO_L12N_T1U_N11_GC_40	IO_L12N_T1U_N11_GC_61	1.2
BA29	DDR4_0_A15	IO_L8P_T1L_N2_AD5P_40	IO_L8P_T1L_N2_AD5P_61	1.2
BE30	DDR4_0_A16	IO_L6N_T0U_N11_AD6N_40	IO_L6N_T0U_N11_AD6N_61	1.2
AV27	DDR4_0_A17	IO_L17N_T2U_N9_AD10N_40	IO_L17N_T2U_N9_AD10N_61	1.2
BE27	DDR4_0_A2	IO_L3P_T0L_N4_AD15P_40	IO_L3P_T0L_N4_AD15P_61	1.2
AV28	DDR4_0_A3	IO_L15P_T2L_N4_AD11P_40	IO_L15P_T2L_N4_AD11P_61	1.2
BB27	DDR4_0_A4	IO_L9P_T1L_N4_AD12P_40	IO_L9P_T1L_N4_AD12P_61	1.2
AT28	DDR4_0_A5	IO_L18N_T2U_N11_AD2N_40	IO_L18N_T2U_N11_AD2N_61	1.2
BC27	DDR4_0_A6	IO_L9N_T1L_N5_AD12N_40	IO_L9N_T1L_N5_AD12N_61	1.2
AY27	DDR4_0_A7	IO_L13P_T2L_N0_GC_QBC_40	IO_L13P_T2L_N0_GC_QBC_61	1.2
BD26	DDR4_0_A8	IO_L1P_T0L_N0_DBC_40	IO_L1P_T0L_N0_DBC_61	1.2
BD28	DDR4_0_A9	IO_L4P_T0U_N6_DBC_AD7P_40	IO_L4P_T0U_N6_DBC_AD7P_61	1.2
BF30	DDR4_0_ACT_N	IO_L2N_T0L_N3_40	IO_L2N_T0L_N3_61	1.2
AN28	DDR4_0_ALERT_N	IO_T3U_N12_40	IO_T3U_N12_61	1.2
BF28	DDR4_0_BA0	IO_L5N_T0U_N9_AD14N_40	IO_L5N_T0U_N9_AD14N_61	1.2
BE28	DDR4_0_BA1	IO_L5P_T0U_N8_AD14P_40	IO_L5P_T0U_N8_AD14P_61	1.2
AU27	DDR4_0_BG0	IO_L17P_T2U_N8_AD10P_40	IO_L17P_T2U_N8_AD10P_61	1.2
BC29	DDR4_0_BG1	IO_T1U_N12_40	IO_T1U_N12_61	1.2
AT27	DDR4_0_C0	IO_L18P_T2U_N10_AD2P_40	IO_L18P_T2U_N10_AD2P_61	1.2
BD30	DDR4_0_C1	IO_L6P_T0U_N10_AD6P_40	IO_L6P_T0U_N10_AD6P_61	1.2
AU29	DDR4_0_C2	IO_L16P_T2U_N6_QBC_AD3P_40	IO_L16P_T2U_N6_QBC_AD3P_61	1.2
BB30	DDR4_0_CK_C	IO_L10N_T1U_N7_QBC_AD4N_40	IO_L10N_T1U_N7_QBC_AD4N_61	1.2
BA30	DDR4_0_CK_T	IO_L10P_T1U_N6_QBC_AD4P_40	IO_L10P_T1U_N6_QBC_AD4P_61	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
BF29	DDR4_0_CKE	IO_L2P_T0L_N2_40	IO_L2P_T0L_N2_61	1.2
BD29	DDR4_0_CS0_N	IO_L4N_T0U_N7_DBC_AD7N_40	IO_L4N_T0U_N7_DBC_AD7N_61	1.2
BC31	DDR4_0_DM0	IO_L7P_T1L_N0_QBC_AD13P_41	IO_L7P_T1L_N0_QBC_AD13P_62	1.2
BE31	DDR4_0_DM1	IO_L1P_T0L_N0_DBC_41	IO_L1P_T0L_N0_DBC_62	1.2
BA32	DDR4_0_DM2	IO_L13P_T2L_N0_GC_QBC_41	IO_L13P_T2L_N0_GC_QBC_62	1.2
BC37	DDR4_0_DM3	IO_L7P_T1L_N0_QBC_AD13P_42	IO_L7P_T1L_N0_QBC_AD13P_63	1.2
AR30	DDR4_0_DM4	IO_L19P_T3L_N0_DBC_AD9P_40	IO_L19P_T3L_N0_DBC_AD9P_61	1.2
BF39	DDR4_0_DM5	IO_L1P_T0L_N0_DBC_42	IO_L1P_T0L_N0_DBC_63	1.2
AP30	DDR4_0_DM6	IO_L19P_T3L_N0_DBC_AD9P_41	IO_L19P_T3L_N0_DBC_AD9P_62	1.2
AY37	DDR4_0_DM7	IO_L13P_T2L_N0_GC_QBC_42	IO_L13P_T2L_N0_GC_QBC_63	1.2
AR35	DDR4_0_DM8	IO_L19P_T3L_N0_DBC_AD9P_42	IO_L19P_T3L_N0_DBC_AD9P_63	1.2
BC33	DDR4_0_DQ0	IO_L9N_T1L_N5_AD12N_41	IO_L9N_T1L_N5_AD12N_62	1.2
BB32	DDR4_0_DQ1	IO_L11N_T1U_N9_GC_41	IO_L11N_T1U_N9_GC_62	1.2
BF35	DDR4_0_DQ10	IO_L2N_T0L_N3_41	IO_L2N_T0L_N3_62	1.2
BF34	DDR4_0_DQ11	IO_L2P_T0L_N2_41	IO_L2P_T0L_N2_62	1.2
BD35	DDR4_0_DQ12	IO_L6N_T0U_N11_AD6N_41	IO_L6N_T0U_N11_AD6N_62	1.2
BF32	DDR4_0_DQ13	IO_L3P_T0L_N4_AD15P_41	IO_L3P_T0L_N4_AD15P_62	1.2
BD34	DDR4_0_DQ14	IO_L6P_T0U_N10_AD6P_41	IO_L6P_T0U_N10_AD6P_62	1.2
BE33	DDR4_0_DQ15	IO_L5N_T0U_N9_AD14N_41	IO_L5N_T0U_N9_AD14N_62	1.2
AV31	DDR4_0_DQ16	IO_L17P_T2U_N8_AD10P_41	IO_L17P_T2U_N8_AD10P_62	1.2
BA35	DDR4_0_DQ17	IO_L14N_T2L_N3_GC_41	IO_L14N_T2L_N3_GC_62	1.2
BA34	DDR4_0_DQ18	IO_L14P_T2L_N2_GC_41	IO_L14P_T2L_N2_GC_62	1.2
AW34	DDR4_0_DQ19	IO_L18N_T2U_N11_AD2N_41	IO_L18N_T2U_N11_AD2N_62	1.2
BB34	DDR4_0_DQ2	IO_L8P_T1L_N2_AD5P_41	IO_L8P_T1L_N2_AD5P_62	1.2
AW31	DDR4_0_DQ20	IO_L15P_T2L_N4_AD11P_41	IO_L15P_T2L_N4_AD11P_62	1.2
AV34	DDR4_0_DQ21	IO_L18P_T2U_N10_AD2P_41	IO_L18P_T2U_N10_AD2P_62	1.2
AY31	DDR4_0_DQ22	IO_L15N_T2L_N5_AD11N_41	IO_L15N_T2L_N5_AD11N_62	1.2
AV32	DDR4_0_DQ23	IO_L17N_T2U_N9_AD10N_41	IO_L17N_T2U_N9_AD10N_62	1.2
BA37	DDR4_0_DQ24	IO_L11P_T1U_N8_GC_42	IO_L11P_T1U_N8_GC_63	1.2
BC40	DDR4_0_DQ25	IO_L9N_T1L_N5_AD12N_42	IO_L9N_T1L_N5_AD12N_63	1.2
BA38	DDR4_0_DQ26	IO_L11N_T1U_N9_GC_42	IO_L11N_T1U_N9_GC_63	1.2
BB40	DDR4_0_DQ27	IO_L8N_T1L_N3_AD5N_42	IO_L8N_T1L_N3_AD5N_63	1.2
AY36	DDR4_0_DQ28	IO_L12N_T1U_N11_GC_42	IO_L12N_T1U_N11_GC_63	1.2
BB39	DDR4_0_DQ29	IO_L8P_T1L_N2_AD5P_42	IO_L8P_T1L_N2_AD5P_63	1.2
AY33	DDR4_0_DQ3	IO_L12N_T1U_N11_GC_41	IO_L12N_T1U_N11_GC_62	1.2
AY35	DDR4_0_DQ30	IO_L12P_T1U_N10_GC_42	IO_L12P_T1U_N10_GC_63	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
BC39	DDR4_0_DQ31	IO_L9P_T1L_N4_AD12P_42	IO_L9P_T1L_N4_AD12P_63	1.2
AP29	DDR4_0_DQ32	IO_L23N_T3U_N9_40	IO_L23N_T3U_N9_61	1.2
AM27	DDR4_0_DQ33	IO_L24P_T3U_N10_40	IO_L24P_T3U_N10_61	1.2
AM29	DDR4_0_DQ34	IO_L20P_T3L_N2_AD1P_40	IO_L20P_T3L_N2_AD1P_61	1.2
AN27	DDR4_0_DQ35	IO_L24N_T3U_N11_40	IO_L24N_T3U_N11_61	1.2
AP28	DDR4_0_DQ36	IO_L23P_T3U_N8_40	IO_L23P_T3U_N8_61	1.2
AR28	DDR4_0_DQ37	IO_L21N_T3L_N5_AD8N_40	IO_L21N_T3L_N5_AD8N_61	1.2
AN29	DDR4_0_DQ38	IO_L20N_T3L_N3_AD1N_40	IO_L20N_T3L_N3_AD1N_61	1.2
AR27	DDR4_0_DQ39	IO_L21P_T3L_N4_AD8P_40	IO_L21P_T3L_N4_AD8P_61	1.2
BC32	DDR4_0_DQ4	IO_L9P_T1L_N4_AD12P_41	IO_L9P_T1L_N4_AD12P_62	1.2
BF41	DDR4_0_DQ40	IO_L3N_T0L_N5_AD15N_42	IO_L3N_T0L_N5_AD15N_63	1.2
BE37	DDR4_0_DQ41	IO_L2P_T0L_N2_42	IO_L2P_T0L_N2_63	1.2
BE40	DDR4_0_DQ42	IO_L3P_T0L_N4_AD15P_42	IO_L3P_T0L_N4_AD15P_63	1.2
BF37	DDR4_0_DQ43	IO_L2N_T0L_N3_42	IO_L2N_T0L_N3_63	1.2
BF42	DDR4_0_DQ44	IO_L5P_T0U_N8_AD14P_42	IO_L5P_T0U_N8_AD14P_63	1.2
BD40	DDR4_0_DQ45	IO_L6N_T0U_N11_AD6N_42	IO_L6N_T0U_N11_AD6N_63	1.2
BF43	DDR4_0_DQ46	IO_L5N_T0U_N9_AD14N_42	IO_L5N_T0U_N9_AD14N_63	1.2
BD39	DDR4_0_DQ47	IO_L6P_T0U_N10_AD6P_42	IO_L6P_T0U_N10_AD6P_63	1.2
AR31	DDR4_0_DQ48	IO_L21P_T3L_N4_AD8P_41	IO_L21P_T3L_N4_AD8P_62	1.2
AL30	DDR4_0_DQ49	IO_L24P_T3U_N10_41	IO_L24P_T3U_N10_62	1.2
BB31	DDR4_0_DQ5	IO_L11P_T1U_N8_GC_41	IO_L11P_T1U_N8_GC_62	1.2
AN32	DDR4_0_DQ50	IO_L20N_T3L_N3_AD1N_41	IO_L20N_T3L_N3_AD1N_62	1.2
AN31	DDR4_0_DQ51	IO_L20P_T3L_N2_AD1P_41	IO_L20P_T3L_N2_AD1P_62	1.2
AR32	DDR4_0_DQ52	IO_L21N_T3L_N5_AD8N_41	IO_L21N_T3L_N5_AD8N_62	1.2
AM30	DDR4_0_DQ53	IO_L24N_T3U_N11_41	IO_L24N_T3U_N11_62	1.2
AU32	DDR4_0_DQ54	IO_L23N_T3U_N9_41	IO_L23N_T3U_N9_62	1.2
AT32	DDR4_0_DQ55	IO_L23P_T3U_N8_41	IO_L23P_T3U_N8_62	1.2
AV37	DDR4_0_DQ56	IO_L15N_T2L_N5_AD11N_42	IO_L15N_T2L_N5_AD11N_63	1.2
AW36	DDR4_0_DQ57	IO_L14N_T2L_N3_GC_42	IO_L14N_T2L_N3_GC_63	1.2
AV38	DDR4_0_DQ58	IO_L17P_T2U_N8_AD10P_42	IO_L17P_T2U_N8_AD10P_63	1.2
AW38	DDR4_0_DQ59	IO_L17N_T2U_N9_AD10N_42	IO_L17N_T2U_N9_AD10N_63	1.2
BC34	DDR4_0_DQ6	IO_L8N_T1L_N3_AD5N_41	IO_L8N_T1L_N3_AD5N_62	1.2
AU36	DDR4_0_DQ60	IO_L18N_T2U_N11_AD2N_42	IO_L18N_T2U_N11_AD2N_63	1.2
AW35	DDR4_0_DQ61	IO_L14P_T2L_N2_GC_42	IO_L14P_T2L_N2_GC_63	1.2
AT36	DDR4_0_DQ62	IO_L18P_T2U_N10_AD2P_42	IO_L18P_T2U_N10_AD2P_63	1.2
AV36	DDR4_0_DQ63	IO_L15P_T2L_N4_AD11P_42	IO_L15P_T2L_N4_AD11P_63	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AP35	DDR4_0_DQ64	IO_L21N_T3L_N5_AD8N_42	IO_L21N_T3L_N5_AD8N_63	1.2
AR36	DDR4_0_DQ65	IO_L23N_T3U_N9_42	IO_L23N_T3U_N9_63	1.2
AP34	DDR4_0_DQ66	IO_L21P_T3L_N4_AD8P_42	IO_L21P_T3L_N4_AD8P_63	1.2
AP36	DDR4_0_DQ67	IO_L23P_T3U_N8_42	IO_L23P_T3U_N8_63	1.2
AP33	DDR4_0_DQ68	IO_L20N_T3L_N3_AD1N_42	IO_L20N_T3L_N3_AD1N_63	1.2
AN36	DDR4_0_DQ69	IO_L24N_T3U_N11_42	IO_L24N_T3U_N11_63	1.2
AY32	DDR4_0_DQ7	IO_L12P_T1U_N10_GC_41	IO_L12P_T1U_N10_GC_62	1.2
AN33	DDR4_0_DQ70	IO_L20P_T3L_N2_AD1P_42	IO_L20P_T3L_N2_AD1P_63	1.2
AN35	DDR4_0_DQ71	IO_L24P_T3U_N10_42	IO_L24P_T3U_N10_63	1.2
BD33	DDR4_0_DQ8	IO_L5P_T0U_N8_AD14P_41	IO_L5P_T0U_N8_AD14P_62	1.2
BF33	DDR4_0_DQ9	IO_L3N_T0L_N5_AD15N_41	IO_L3N_T0L_N5_AD15N_62	1.2
BB36	DDR4_0_DQS0_C	IO_L10N_T1U_N7_QBC_AD4N_41	IO_L10N_T1U_N7_QBC_AD4N_62	1.2
BB35	DDR4_0_DQS0_T	IO_L10P_T1U_N6_QBC_AD4P_41	IO_L10P_T1U_N6_QBC_AD4P_62	1.2
BE36	DDR4_0_DQS1_C	IO_L4N_T0U_N7_DBC_AD7N_41	IO_L4N_T0U_N7_DBC_AD7N_62	1.2
BE35	DDR4_0_DQS1_T	IO_L4P_T0U_N6_DBC_AD7P_41	IO_L4P_T0U_N6_DBC_AD7P_62	1.2
AW33	DDR4_0_DQS2_C	IO_L16N_T2U_N7_QBC_AD3N_41	IO_L16N_T2U_N7_QBC_AD3N_62	1.2
AV33	DDR4_0_DQS2_T	IO_L16P_T2U_N6_QBC_AD3P_41	IO_L16P_T2U_N6_QBC_AD3P_62	1.2
BA40	DDR4_0_DQS3_C	IO_L10N_T1U_N7_QBC_AD4N_42	IO_L10N_T1U_N7_QBC_AD4N_63	1.2
BA39	DDR4_0_DQS3_T	IO_L10P_T1U_N6_QBC_AD4P_42	IO_L10P_T1U_N6_QBC_AD4P_63	1.2
AL29	DDR4_0_DQS4_C	IO_L22N_T3U_N7_DBC_AD0N_40	IO_L22N_T3U_N7_DBC_AD0N_61	1.2
AL28	DDR4_0_DQS4_T	IO_L22P_T3U_N6_DBC_AD0P_40	IO_L22P_T3U_N6_DBC_AD0P_61	1.2
BF38	DDR4_0_DQS5_C	IO_L4N_T0U_N7_DBC_AD7N_42	IO_L4N_T0U_N7_DBC_AD7N_63	1.2
BE38	DDR4_0_DQS5_T	IO_L4P_T0U_N6_DBC_AD7P_42	IO_L4P_T0U_N6_DBC_AD7P_63	1.2
AM32	DDR4_0_DQS6_C	IO_L22N_T3U_N7_DBC_AD0N_41	IO_L22N_T3U_N7_DBC_AD0N_62	1.2
AM31	DDR4_0_DQS6_T	IO_L22P_T3U_N6_DBC_AD0P_41	IO_L22P_T3U_N6_DBC_AD0P_62	1.2
AU35	DDR4_0_DQS7_C	IO_L16N_T2U_N7_QBC_AD3N_42	IO_L16N_T2U_N7_QBC_AD3N_63	1.2
AU34	DDR4_0_DQS7_T	IO_L16P_T2U_N6_QBC_AD3P_42	IO_L16P_T2U_N6_QBC_AD3P_63	1.2
AN34	DDR4_0_DQS8_C	IO_L22N_T3U_N7_DBC_AD0N_42	IO_L22N_T3U_N7_DBC_AD0N_63	1.2
AM34	DDR4_0_DQS8_T	IO_L22P_T3U_N6_DBC_AD0P_42	IO_L22P_T3U_N6_DBC_AD0P_63	1.2
AW30	DDR4_0_ODT	IO_L14P_T2L_N2_GC_40	IO_L14P_T2L_N2_GC_61	1.2
AV29	DDR4_0_PAR	IO_L15N_T2L_N5_AD11N_40	IO_L15N_T2L_N5_AD11N_61	1.2
BF27	DDR4_0_RESET_N	IO_L3N_T0L_N5_AD15N_40	IO_L3N_T0L_N5_AD15N_61	1.2
AY30	DDR4_0_TEN	IO_L14N_T2L_N3_GC_40	IO_L14N_T2L_N3_GC_61	1.2
BC23	DDR4_1_A0	IO_L2P_T0L_N2_FOE_B_65	IO_L2P_T0L_N2_FOE_B_65	1.2
BD23	DDR4_1_A1	IO_L2N_T0L_N3_FWE_FCS2_B_65	IO_L2N_T0L_N3_FWE_FCS2_B_65	1.2
BB24	DDR4_1_A10	IO_L9P_T1L_N4_AD12P_A14_D30_65	IO_L9P_T1L_N4_AD12P_A14_D30_65	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
BB25	DDR4_1_A11	IO_L9N_T1L_N5_AD12N_A15_D31_65	IO_L9N_T1L_N5_AD12N_A15_D31_65	1.2
BC22	DDR4_1_A12	IO_L7N_T1L_N1_QBC_AD13N_-A19_65	IO_L7N_T1L_N1_QBC_AD13N_-A19_65	1.2
BF25	DDR4_1_A13	IO_L5N_T0U_N9_AD14N_A23_65	IO_L5N_T0U_N9_AD14N_A23_65	1.2
BD24	DDR4_1_A14	IO_L4N_T0U_N7_DBC_AD7N_A25_65	IO_L4N_T0U_N7_DBC_AD7N_A25_65	1.2
AN23	DDR4_1_A15	IO_L19P_T3L_N0_DBC_AD9P_D10_65	IO_L19P_T3L_N0_DBC_AD9P_D10_65	1.2
AR26	DDR4_1_A16	IO_L23N_T3U_N9_PERSTN1_I2-C_SDA_65	IO_L23N_T3U_N9_PERSTN1_I2-C_SDA_65	1.2
BF22	DDR4_1_A17	IO_L1N_T0L_N1_DBC_RS1_65	IO_L1N_T0L_N1_DBC_RS1_65	1.2
AN26	DDR4_1_A2	IO_L24N_T3U_N11_DOUT_CSO_B_65	IO_L24N_T3U_N11_DOUT_CSO_B_65	1.2
AN24	DDR4_1_A3	IO_L19N_T3L_N1_DBC_AD9N_-D11_65	IO_L19N_T3L_N1_DBC_AD9N_-D11_65	1.2
AM25	DDR4_1_A4	IO_L22N_T3U_N7_DBC_AD0N_-D05_65	IO_L22N_T3U_N7_DBC_AD0N_-D05_65	1.2
BF24	DDR4_1_A5	IO_L5P_T0U_N8_AD14P_A22_65	IO_L5P_T0U_N8_AD14P_A22_65	1.2
BA23	DDR4_1_A6	IO_L8N_T1L_N3_AD5N_A17_65	IO_L8N_T1L_N3_AD5N_A17_65	1.2
BA25	DDR4_1_A7	IO_T1U_N12_SMBALERT_65	IO_T1U_N12_SMBALERT_65	1.2
BE25	DDR4_1_A8	IO_L6N_T0U_N11_AD6N_A21_65	IO_L6N_T0U_N11_AD6N_A21_65	1.2
AP25	DDR4_1_A9	IO_T2U_N12_CSI_ADV_B_65	IO_T2U_N12_CSI_ADV_B_65	1.2
AP23	DDR4_1_ACT_N	IO_L21P_T3L_N4_AD8P_D06_65	IO_L21P_T3L_N4_AD8P_D06_65	1.2
AL24	DDR4_1_ALERT_N	IO_L20P_T3L_N2_AD1P_D08_65	IO_L20P_T3L_N2_AD1P_D08_65	1.2
BD25	DDR4_1_BA0	IO_L6P_T0U_N10_AD6P_A20_65	IO_L6P_T0U_N10_AD6P_A20_65	1.2
AW24	DDR4_1_BA1	IO_L12N_T1U_N11_GC_A09_D25_65	IO_L12N_T1U_N11_GC_A09_D25_65	1.2
AW23	DDR4_1_BG0	IO_L12P_T1U_N10_GC_A08_D24_65	IO_L12P_T1U_N10_GC_A08_D24_65	1.2
BF23	DDR4_1_BG1	IO_L3N_T0L_N5_AD15N_A27_65	IO_L3N_T0L_N5_AD15N_A27_65	1.2
AR25	DDR4_1_C0	IO_L23P_T3U_N8_I2C_SCLK_65	IO_L23P_T3U_N8_I2C_SCLK_65	1.2
BE23	DDR4_1_C1	IO_L3P_T0L_N4_AD15P_A26_65	IO_L3P_T0L_N4_AD15P_A26_65	1.2
BC24	DDR4_1_C2	IO_L4P_T0U_N6_DBC_AD7P_A24_65	IO_L4P_T0U_N6_DBC_AD7P_A24_65	1.2
AY23	DDR4_1_CK_C	IO_L10N_T1U_N7_QBC_AD4N_-A13_D29_65	IO_L10N_T1U_N7_QBC_AD4N_-A13_D29_65	1.2
AY22	DDR4_1_CK_T	IO_L10P_T1U_N6_QBC_AD4P_-A12_D28_65	IO_L10P_T1U_N6_QBC_AD4P_-A12_D28_65	1.2
BA22	DDR4_1_CKE	IO_L8P_T1L_N2_AD5P_A16_65	IO_L8P_T1L_N2_AD5P_A16_65	1.2
BB22	DDR4_1_CS0_N	IO_L7P_T1L_N0_QBC_AD13P_A18_65	IO_L7P_T1L_N0_QBC_AD13P_A18_65	1.2
AW25	DDR4_1_DM0	IO_L13P_T2L_N0_GC_QBC_A0-6_D22_65	IO_L13P_T2L_N0_GC_QBC_A0-6_D22_65	1.2
BE15	DDR4_1_DM1	IO_L1P_T0L_N0_DBC_66	IO_L1P_T0L_N0_DBC_66	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AW16	DDR4_1_DM2	IO_L13P_T2L_N0_GC_QBC_66	IO_L13P_T2L_N0_GC_QBC_66	1.2
BB14	DDR4_1_DM3	IO_L7P_T1L_N0_QBC_AD13P_66	IO_L7P_T1L_N0_QBC_AD13P_66	1.2
AY13	DDR4_1_DM4	IO_L13P_T2L_N0_GC_QBC_67	IO_L13P_T2L_N0_GC_QBC_67	1.2
BE8	DDR4_1_DM5	IO_L1P_T0L_N0_DBC_67	IO_L1P_T0L_N0_DBC_67	1.2
AM17	DDR4_1_DM6	IO_L19P_T3L_N0_DBC_AD9P_66	IO_L19P_T3L_N0_DBC_AD9P_66	1.2
BA10	DDR4_1_DM7	IO_L7P_T1L_N0_QBC_AD13P_67	IO_L7P_T1L_N0_QBC_AD13P_67	1.2
AN14	DDR4_1_DM8	IO_L19P_T3L_N0_DBC_AD9P_67	IO_L19P_T3L_N0_DBC_AD9P_67	1.2
AV24	DDR4_1_DQ0	IO_L14N_T2L_N3_GC_A05_D21_65	IO_L14N_T2L_N3_GC_A05_D21_65	1.2
AV26	DDR4_1_DQ1	IO_L17N_T2U_N9_AD10N_D15_65	IO_L17N_T2U_N9_AD10N_D15_65	1.2
BF12	DDR4_1_DQ10	IO_L6N_T0U_N11_AD6N_66	IO_L6N_T0U_N11_AD6N_66	1.2
BD14	DDR4_1_DQ11	IO_L5P_T0U_N8_AD14P_66	IO_L5P_T0U_N8_AD14P_66	1.2
BF13	DDR4_1_DQ12	IO_L2N_T0L_N3_66	IO_L2N_T0L_N3_66	1.2
BD15	DDR4_1_DQ13	IO_L3N_T0L_N5_AD15N_66	IO_L3N_T0L_N5_AD15N_66	1.2
BF14	DDR4_1_DQ14	IO_L2P_T0L_N2_66	IO_L2P_T0L_N2_66	1.2
BD16	DDR4_1_DQ15	IO_L3P_T0L_N4_AD15P_66	IO_L3P_T0L_N4_AD15P_66	1.2
AT17	DDR4_1_DQ16	IO_L15N_T2L_N5_AD11N_66	IO_L15N_T2L_N5_AD11N_66	1.2
BB17	DDR4_1_DQ17	IO_L14P_T2L_N2_GC_66	IO_L14P_T2L_N2_GC_66	1.2
AU16	DDR4_1_DQ18	IO_L17N_T2U_N9_AD10N_66	IO_L17N_T2U_N9_AD10N_66	1.2
AV16	DDR4_1_DQ19	IO_L18N_T2U_N11_AD2N_66	IO_L18N_T2U_N11_AD2N_66	1.2
AV23	DDR4_1_DQ2	IO_L14P_T2L_N2_GC_A04_D20_65	IO_L14P_T2L_N2_GC_A04_D20_65	1.2
AT18	DDR4_1_DQ20	IO_L15P_T2L_N4_AD11P_66	IO_L15P_T2L_N4_AD11P_66	1.2
BB16	DDR4_1_DQ21	IO_L14N_T2L_N3_GC_66	IO_L14N_T2L_N3_GC_66	1.2
AU17	DDR4_1_DQ22	IO_L17P_T2U_N8_AD10P_66	IO_L17P_T2U_N8_AD10P_66	1.2
AV17	DDR4_1_DQ23	IO_L18P_T2U_N10_AD2P_66	IO_L18P_T2U_N10_AD2P_66	1.2
AY17	DDR4_1_DQ24	IO_L11N_T1U_N9_GC_66	IO_L11N_T1U_N9_GC_66	1.2
BD11	DDR4_1_DQ25	IO_L8N_T1L_N3_AD5N_66	IO_L8N_T1L_N3_AD5N_66	1.2
BA17	DDR4_1_DQ26	IO_L12N_T1U_N11_GC_66	IO_L12N_T1U_N11_GC_66	1.2
BA15	DDR4_1_DQ27	IO_L9P_T1L_N4_AD12P_66	IO_L9P_T1L_N4_AD12P_66	1.2
BA18	DDR4_1_DQ28	IO_L12P_T1U_N10_GC_66	IO_L12P_T1U_N10_GC_66	1.2
BC11	DDR4_1_DQ29	IO_L8P_T1L_N2_AD5P_66	IO_L8P_T1L_N2_AD5P_66	1.2
AU25	DDR4_1_DQ3	IO_L15N_T2L_N5_AD11N_A03_-D19_65	IO_L15N_T2L_N5_AD11N_A03_-D19_65	1.2
AY18	DDR4_1_DQ30	IO_L11P_T1U_N8_GC_66	IO_L11P_T1U_N8_GC_66	1.2
BB15	DDR4_1_DQ31	IO_L9N_T1L_N5_AD12N_66	IO_L9N_T1L_N5_AD12N_66	1.2
AU13	DDR4_1_DQ32	IO_L17P_T2U_N8_AD10P_67	IO_L17P_T2U_N8_AD10P_67	1.2
BA11	DDR4_1_DQ33	IO_L14N_T2L_N3_GC_67	IO_L14N_T2L_N3_GC_67	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AV13	DDR4_1_DQ34	IO_L17N_T2U_N9_AD10N_67	IO_L17N_T2U_N9_AD10N_67	1.2
AY11	DDR4_1_DQ35	IO_L14P_T2L_N2_GC_67	IO_L14P_T2L_N2_GC_67	1.2
AU14	DDR4_1_DQ36	IO_L15P_T2L_N4_AD11P_67	IO_L15P_T2L_N4_AD11P_67	1.2
AW13	DDR4_1_DQ37	IO_L18N_T2U_N11_AD2N_67	IO_L18N_T2U_N11_AD2N_67	1.2
AV14	DDR4_1_DQ38	IO_L15N_T2L_N5_AD11N_67	IO_L15N_T2L_N5_AD11N_67	1.2
AW14	DDR4_1_DQ39	IO_L18P_T2U_N10_AD2P_67	IO_L18P_T2U_N10_AD2P_67	1.2
AU24	DDR4_1_DQ4	IO_L18N_T2U_N11_AD2N_D13_65	IO_L18N_T2U_N11_AD2N_D13_65	1.2
BD8	DDR4_1_DQ40	IO_L6N_T0U_N11_AD6N_67	IO_L6N_T0U_N11_AD6N_67	1.2
BC7	DDR4_1_DQ41	IO_L5P_T0U_N8_AD14P_67	IO_L5P_T0U_N8_AD14P_67	1.2
BE10	DDR4_1_DQ42	IO_L2N_T0L_N3_67	IO_L2N_T0L_N3_67	1.2
BF7	DDR4_1_DQ43	IO_L3N_T0L_N5_AD15N_67	IO_L3N_T0L_N5_AD15N_67	1.2
BD10	DDR4_1_DQ44	IO_L2P_T0L_N2_67	IO_L2P_T0L_N2_67	1.2
BE7	DDR4_1_DQ45	IO_L3P_T0L_N4_AD15P_67	IO_L3P_T0L_N4_AD15P_67	1.2
BD9	DDR4_1_DQ46	IO_L6P_T0U_N10_AD6P_67	IO_L6P_T0U_N10_AD6P_67	1.2
BD7	DDR4_1_DQ47	IO_L5N_T0U_N9_AD14N_67	IO_L5N_T0U_N9_AD14N_67	1.2
AL16	DDR4_1_DQ48	IO_L21N_T3L_N5_AD8N_66	IO_L21N_T3L_N5_AD8N_66	1.2
AN16	DDR4_1_DQ49	IO_L24N_T3U_N11_66	IO_L24N_T3U_N11_66	1.2
AU26	DDR4_1_DQ5	IO_L17P_T2U_N8_AD10P_D14_65	IO_L17P_T2U_N8_AD10P_D14_65	1.2
AM15	DDR4_1_DQ50	IO_L23N_T3U_N9_66	IO_L23N_T3U_N9_66	1.2
AN17	DDR4_1_DQ51	IO_L24P_T3U_N10_66	IO_L24P_T3U_N10_66	1.2
AL17	DDR4_1_DQ52	IO_L21P_T3L_N4_AD8P_66	IO_L21P_T3L_N4_AD8P_66	1.2
AR18	DDR4_1_DQ53	IO_L20N_T3L_N3_AD1N_66	IO_L20N_T3L_N3_AD1N_66	1.2
AL15	DDR4_1_DQ54	IO_L23P_T3U_N8_66	IO_L23P_T3U_N8_66	1.2
AP18	DDR4_1_DQ55	IO_L20P_T3L_N2_AD1P_66	IO_L20P_T3L_N2_AD1P_66	1.2
BA8	DDR4_1_DQ56	IO_L9P_T1L_N4_AD12P_67	IO_L9P_T1L_N4_AD12P_67	1.2
BB12	DDR4_1_DQ57	IO_L12N_T1U_N11_GC_67	IO_L12N_T1U_N11_GC_67	1.2
BA7	DDR4_1_DQ58	IO_L9N_T1L_N5_AD12N_67	IO_L9N_T1L_N5_AD12N_67	1.2
BA12	DDR4_1_DQ59	IO_L12P_T1U_N10_GC_67	IO_L12P_T1U_N10_GC_67	1.2
AT24	DDR4_1_DQ6	IO_L18P_T2U_N10_AD2P_D12_65	IO_L18P_T2U_N10_AD2P_D12_65	1.2
BC9	DDR4_1_DQ60	IO_L8N_T1L_N3_AD5N_67	IO_L8N_T1L_N3_AD5N_67	1.2
BA14	DDR4_1_DQ61	IO_L11P_T1U_N8_GC_67	IO_L11P_T1U_N8_GC_67	1.2
BB9	DDR4_1_DQ62	IO_L8P_T1L_N2_AD5P_67	IO_L8P_T1L_N2_AD5P_67	1.2
BA13	DDR4_1_DQ63	IO_L11N_T1U_N9_GC_67	IO_L11N_T1U_N9_GC_67	1.2
AP13	DDR4_1_DQ64	IO_L24P_T3U_N10_67	IO_L24P_T3U_N10_67	1.2
AT15	DDR4_1_DQ65	IO_L20N_T3L_N3_AD1N_67	IO_L20N_T3L_N3_AD1N_67	1.2
AR13	DDR4_1_DQ66	IO_L24N_T3U_N11_67	IO_L24N_T3U_N11_67	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AR15	DDR4_1_DQ67	IO_L20P_T3L_N2_AD1P_67	IO_L20P_T3L_N2_AD1P_67	1.2
AN13	DDR4_1_DQ68	IO_L23N_T3U_N9_67	IO_L23N_T3U_N9_67	1.2
AM14	DDR4_1_DQ69	IO_L21N_T3L_N5_AD8N_67	IO_L21N_T3L_N5_AD8N_67	1.2
AT25	DDR4_1_DQ7	IO_L15P_T2L_N4_AD11P_A02_-D18_65	IO_L15P_T2L_N4_AD11P_A02_-D18_65	1.2
AM13	DDR4_1_DQ70	IO_L23P_T3U_N8_67	IO_L23P_T3U_N8_67	1.2
AL14	DDR4_1_DQ71	IO_L21P_T3L_N4_AD8P_67	IO_L21P_T3L_N4_AD8P_67	1.2
BE13	DDR4_1_DQ8	IO_L6P_T0U_N10_AD6P_66	IO_L6P_T0U_N10_AD6P_66	1.2
BD13	DDR4_1_DQ9	IO_L5N_T0U_N9_AD14N_66	IO_L5N_T0U_N9_AD14N_66	1.2
AT23	DDR4_1_DQS0_C	IO_L16N_T2U_N7_QBC_AD3N_-A01_D17_65	IO_L16N_T2U_N7_QBC_AD3N_-A01_D17_65	1.2
AR23	DDR4_1_DQS0_T	IO_L16P_T2U_N6_QBC_AD3P_-A00_D16_65	IO_L16P_T2U_N6_QBC_AD3P_-A00_D16_65	1.2
BE11	DDR4_1_DQS1_C	IO_L4N_T0U_N7_DBC_AD7N_66	IO_L4N_T0U_N7_DBC_AD7N_66	1.2
BE12	DDR4_1_DQS1_T	IO_L4P_T0U_N6_DBC_AD7P_66	IO_L4P_T0U_N6_DBC_AD7P_66	1.2
AW18	DDR4_1_DQS2_C	IO_L16N_T2U_N7_QBC_AD3N_66	IO_L16N_T2U_N7_QBC_AD3N_66	1.2
AV18	DDR4_1_DQS2_T	IO_L16P_T2U_N6_QBC_AD3P_66	IO_L16P_T2U_N6_QBC_AD3P_66	1.2
BC12	DDR4_1_DQS3_C	IO_L10N_T1U_N7_QBC_AD4N_66	IO_L10N_T1U_N7_QBC_AD4N_66	1.2
BC13	DDR4_1_DQS3_T	IO_L10P_T1U_N6_QBC_AD4P_66	IO_L10P_T1U_N6_QBC_AD4P_66	1.2
AY15	DDR4_1_DQS4_C	IO_L16N_T2U_N7_QBC_AD3N_67	IO_L16N_T2U_N7_QBC_AD3N_67	1.2
AW15	DDR4_1_DQS4_T	IO_L16P_T2U_N6_QBC_AD3P_67	IO_L16P_T2U_N6_QBC_AD3P_67	1.2
BF9	DDR4_1_DQS5_C	IO_L4N_T0U_N7_DBC_AD7N_67	IO_L4N_T0U_N7_DBC_AD7N_67	1.2
BF10	DDR4_1_DQS5_T	IO_L4P_T0U_N6_DBC_AD7P_67	IO_L4P_T0U_N6_DBC_AD7P_67	1.2
AR16	DDR4_1_DQS6_C	IO_L22N_T3U_N7_DBC_AD0N_66	IO_L22N_T3U_N7_DBC_AD0N_66	1.2
AP16	DDR4_1_DQS6_T	IO_L22P_T3U_N6_DBC_AD0P_66	IO_L22P_T3U_N6_DBC_AD0P_66	1.2
BB10	DDR4_1_DQS7_C	IO_L10N_T1U_N7_QBC_AD4N_67	IO_L10N_T1U_N7_QBC_AD4N_67	1.2
BB11	DDR4_1_DQS7_T	IO_L10P_T1U_N6_QBC_AD4P_67	IO_L10P_T1U_N6_QBC_AD4P_67	1.2
AT13	DDR4_1_DQS8_C	IO_L22N_T3U_N7_DBC_AD0N_67	IO_L22N_T3U_N7_DBC_AD0N_67	1.2
AT14	DDR4_1_DQS8_T	IO_L22P_T3U_N6_DBC_AD0P_67	IO_L22P_T3U_N6_DBC_AD0P_67	1.2
AM24	DDR4_1_ODT	IO_L20N_T3L_N3_AD1N_D09_65	IO_L20N_T3L_N3_AD1N_D09_65	1.2
BE22	DDR4_1_PAR	IO_L1P_T0L_N0_DBC_RS0_65	IO_L1P_T0L_N0_DBC_RS0_65	1.2
AL25	DDR4_1_RESET_N	IO_L22P_T3U_N6_DBC_AD0P_-D04_65	IO_L22P_T3U_N6_DBC_AD0P_-D04_65	1.2
AP24	DDR4_1_TEN	IO_L21N_T3L_N5_AD8N_D07_65	IO_L21N_T3L_N5_AD8N_D07_65	1.2
B24	DDR4_2_A0	IO_L23N_T3U_N9_72	IO_L23N_T3U_N9_74	1.2
B25	DDR4_2_A1	IO_L23P_T3U_N8_72	IO_L23P_T3U_N8_74	1.2
A23	DDR4_2_A10	IO_L24P_T3U_N10_72	IO_L24P_T3U_N10_74	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
G25	DDR4_2_A11	IO_L14P_T2L_N2_GC_72	IO_L14P_T2L_N2_GC_74	1.2
C24	DDR4_2_A12	IO_L21P_T3L_N4_AD8P_72	IO_L21P_T3L_N4_AD8P_74	1.2
L24	DDR4_2_A13	IO_L9P_T1L_N4_AD12P_72	IO_L9P_T1L_N4_AD12P_74	1.2
K22	DDR4_2_A14	IO_L8P_T1L_N2_AD5P_72	IO_L8P_T1L_N2_AD5P_74	1.2
C22	DDR4_2_A15	IO_L20P_T3L_N2_AD1P_72	IO_L20P_T3L_N2_AD1P_74	1.2
G22	DDR4_2_A16	IO_L18P_T2U_N10_AD2P_72	IO_L18P_T2U_N10_AD2P_74	1.2
D25	DDR4_2_A17	IO_T2U_N12_72	IO_T2U_N12_74	1.2
F25	DDR4_2_A2	IO_L15P_T2L_N4_AD11P_72	IO_L15P_T2L_N4_AD11P_74	1.2
D23	DDR4_2_A3	IO_L19N_T3L_N1_DBC_AD9N_72	IO_L19N_T3L_N1_DBC_AD9N_74	1.2
D24	DDR4_2_A4	IO_L19P_T3L_N0_DBC_AD9P_72	IO_L19P_T3L_N0_DBC_AD9P_74	1.2
H23	DDR4_2_A5	IO_L13P_T2L_N0_GC_QBC_72	IO_L13P_T2L_N0_GC_QBC_74	1.2
F23	DDR4_2_A6	IO_L16P_T2U_N6_QBC_AD3P_72	IO_L16P_T2U_N6_QBC_AD3P_74	1.2
F24	DDR4_2_A7	IO_L14N_T2L_N3_GC_72	IO_L14N_T2L_N3_GC_74	1.2
G24	DDR4_2_A8	IO_L12N_T1U_N11_GC_72	IO_L12N_T1U_N11_GC_74	1.2
E25	DDR4_2_A9	IO_L15N_T2L_N5_AD11N_72	IO_L15N_T2L_N5_AD11N_74	1.2
C23	DDR4_2_ACT_N	IO_L21N_T3L_N5_AD8N_72	IO_L21N_T3L_N5_AD8N_74	1.2
L22	DDR4_2_ALERT_N	IO_L7N_T1L_N1_QBC_AD13N_72	IO_L7N_T1L_N1_QBC_AD13N_74	1.2
K23	DDR4_2_BA0	IO_T1U_N12_72	IO_T1U_N12_74	1.2
E23	DDR4_2_BA1	IO_L16N_T2U_N7_QBC_AD3N_72	IO_L16N_T2U_N7_QBC_AD3N_74	1.2
F22	DDR4_2_BG0	IO_L17P_T2U_N8_AD10P_72	IO_L17P_T2U_N8_AD10P_74	1.2
H22	DDR4_2_BG1	IO_L13N_T2L_N1_GC_QBC_72	IO_L13N_T2L_N1_GC_QBC_74	1.2
E21	DDR4_2_C0	IO_T3U_N12_72	IO_T3U_N12_74	1.2
L23	DDR4_2_C1	IO_L9N_T1L_N5_AD12N_72	IO_L9N_T1L_N5_AD12N_74	1.2
K21	DDR4_2_C2	IO_L8N_T1L_N3_AD5N_72	IO_L8N_T1L_N3_AD5N_74	1.2
H21	DDR4_2_CK_C	IO_L10N_T1U_N7_QBC_AD4N_72	IO_L10N_T1U_N7_QBC_AD4N_74	1.2
J21	DDR4_2_CK_T	IO_L10P_T1U_N6_QBC_AD4P_72	IO_L10P_T1U_N6_QBC_AD4P_74	1.2
A22	DDR4_2_CKE	IO_L24N_T3U_N11_72	IO_L24N_T3U_N11_74	1.2
B22	DDR4_2_CS0_N	IO_L20N_T3L_N3_AD1N_72	IO_L20N_T3L_N3_AD1N_74	1.2
N22	DDR4_2_DM0	IO_L1P_T0L_N0_DBC_72	IO_L1P_T0L_N0_DBC_74	1.2
B19	DDR4_2_DM1	IO_L19P_T3L_N0_DBC_AD9P_71	IO_L19P_T3L_N0_DBC_AD9P_73	1.2
H19	DDR4_2_DM2	IO_L13P_T2L_N0_GC_QBC_71	IO_L13P_T2L_N0_GC_QBC_73	1.2
K18	DDR4_2_DM3	IO_L7P_T1L_N0_QBC_AD13P_71	IO_L7P_T1L_N0_QBC_AD13P_73	1.2
N17	DDR4_2_DM4	IO_L1P_T0L_N0_DBC_71	IO_L1P_T0L_N0_DBC_73	1.2
B14	DDR4_2_DM5	IO_L19P_T3L_N0_DBC_AD9P_70	IO_L19P_T3L_N0_DBC_AD9P_72	1.2
J16	DDR4_2_DM6	IO_L13P_T2L_N0_GC_QBC_70	IO_L13P_T2L_N0_GC_QBC_72	1.2
L15	DDR4_2_DM7	IO_L7P_T1L_N0_QBC_AD13P_70	IO_L7P_T1L_N0_QBC_AD13P_72	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
T13	DDR4_2_DM8	IO_L1P_T0L_N0_DBC_70	IO_L1P_T0L_N0_DBC_72	1.2
P23	DDR4_2_DQ0	IO_L3P_T0L_N4_AD15P_72	IO_L3P_T0L_N4_AD15P_74	1.2
P21	DDR4_2_DQ1	IO_L2N_T0L_N3_72	IO_L2N_T0L_N3_74	1.2
A18	DDR4_2_DQ10	IO_L20P_T3L_N2_AD1P_71	IO_L20P_T3L_N2_AD1P_73	1.2
A20	DDR4_2_DQ11	IO_L21N_T3L_N5_AD8N_71	IO_L21N_T3L_N5_AD8N_73	1.2
C18	DDR4_2_DQ12	IO_L24N_T3U_N11_71	IO_L24N_T3U_N11_73	1.2
C21	DDR4_2_DQ13	IO_L23P_T3U_N8_71	IO_L23P_T3U_N8_73	1.2
C19	DDR4_2_DQ14	IO_L24P_T3U_N10_71	IO_L24P_T3U_N10_73	1.2
B21	DDR4_2_DQ15	IO_L23N_T3U_N9_71	IO_L23N_T3U_N9_73	1.2
D20	DDR4_2_DQ16	IO_L15P_T2L_N4_AD11P_71	IO_L15P_T2L_N4_AD11P_73	1.2
H18	DDR4_2_DQ17	IO_L14N_T2L_N3_GC_71	IO_L14N_T2L_N3_GC_73	1.2
D19	DDR4_2_DQ18	IO_L15N_T2L_N5_AD11N_71	IO_L15N_T2L_N5_AD11N_73	1.2
E18	DDR4_2_DQ19	IO_L18P_T2U_N10_AD2P_71	IO_L18P_T2U_N10_AD2P_73	1.2
N23	DDR4_2_DQ2	IO_L3N_T0L_N5_AD15N_72	IO_L3N_T0L_N5_AD15N_74	1.2
E20	DDR4_2_DQ20	IO_L17N_T2U_N9_AD10N_71	IO_L17N_T2U_N9_AD10N_73	1.2
J18	DDR4_2_DQ21	IO_L14P_T2L_N2_GC_71	IO_L14P_T2L_N2_GC_73	1.2
F20	DDR4_2_DQ22	IO_L17P_T2U_N8_AD10P_71	IO_L17P_T2U_N8_AD10P_73	1.2
E17	DDR4_2_DQ23	IO_L18N_T2U_N11_AD2N_71	IO_L18N_T2U_N11_AD2N_73	1.2
J19	DDR4_2_DQ24	IO_L9N_T1L_N5_AD12N_71	IO_L9N_T1L_N5_AD12N_73	1.2
G20	DDR4_2_DQ25	IO_L11P_T1U_N8_GC_71	IO_L11P_T1U_N8_GC_73	1.2
G17	DDR4_2_DQ26	IO_L12N_T1U_N11_GC_71	IO_L12N_T1U_N11_GC_73	1.2
H17	DDR4_2_DQ27	IO_L12P_T1U_N10_GC_71	IO_L12P_T1U_N10_GC_73	1.2
L19	DDR4_2_DQ28	IO_L8P_T1L_N2_AD5P_71	IO_L8P_T1L_N2_AD5P_73	1.2
F19	DDR4_2_DQ29	IO_L11N_T1U_N9_GC_71	IO_L11N_T1U_N9_GC_73	1.2
R21	DDR4_2_DQ3	IO_L2P_T0L_N2_72	IO_L2P_T0L_N2_74	1.2
L18	DDR4_2_DQ30	IO_L8N_T1L_N3_AD5N_71	IO_L8N_T1L_N3_AD5N_73	1.2
J20	DDR4_2_DQ31	IO_L9P_T1L_N4_AD12P_71	IO_L9P_T1L_N4_AD12P_73	1.2
N19	DDR4_2_DQ32	IO_L3P_T0L_N4_AD15P_71	IO_L3P_T0L_N4_AD15P_73	1.2
R17	DDR4_2_DQ33	IO_L6N_T0U_N11_AD6N_71	IO_L6N_T0U_N11_AD6N_73	1.2
N18	DDR4_2_DQ34	IO_L3N_T0L_N5_AD15N_71	IO_L3N_T0L_N5_AD15N_73	1.2
R18	DDR4_2_DQ35	IO_L6P_T0U_N10_AD6P_71	IO_L6P_T0U_N10_AD6P_73	1.2
M19	DDR4_2_DQ36	IO_L5N_T0U_N9_AD14N_71	IO_L5N_T0U_N9_AD14N_73	1.2
R20	DDR4_2_DQ37	IO_L2N_T0L_N3_71	IO_L2N_T0L_N3_73	1.2
M20	DDR4_2_DQ38	IO_L5P_T0U_N8_AD14P_71	IO_L5P_T0U_N8_AD14P_73	1.2
T20	DDR4_2_DQ39	IO_L2P_T0L_N2_71	IO_L2P_T0L_N2_73	1.2
N24	DDR4_2_DQ4	IO_L5N_T0U_N9_AD14N_72	IO_L5N_T0U_N9_AD14N_74	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
B13	DDR4_2_DQ40	IO_L24P_T3U_N10_70	IO_L24P_T3U_N10_72	1.2
B15	DDR4_2_DQ41	IO_L21P_T3L_N4_AD8P_70	IO_L21P_T3L_N4_AD8P_72	1.2
A13	DDR4_2_DQ42	IO_L24N_T3U_N11_70	IO_L24N_T3U_N11_72	1.2
A15	DDR4_2_DQ43	IO_L21N_T3L_N5_AD8N_70	IO_L21N_T3L_N5_AD8N_72	1.2
C14	DDR4_2_DQ44	IO_L20N_T3L_N3_AD1N_70	IO_L20N_T3L_N3_AD1N_72	1.2
B16	DDR4_2_DQ45	IO_L23N_T3U_N9_70	IO_L23N_T3U_N9_72	1.2
D14	DDR4_2_DQ46	IO_L20P_T3L_N2_AD1P_70	IO_L20P_T3L_N2_AD1P_72	1.2
C16	DDR4_2_DQ47	IO_L23P_T3U_N8_70	IO_L23P_T3U_N8_72	1.2
F15	DDR4_2_DQ48	IO_L18P_T2U_N10_AD2P_70	IO_L18P_T2U_N10_AD2P_72	1.2
H14	DDR4_2_DQ49	IO_L14P_T2L_N2_GC_70	IO_L14P_T2L_N2_GC_72	1.2
R23	DDR4_2_DQ5	IO_L6N_T0U_N11_AD6N_72	IO_L6N_T0U_N11_AD6N_74	1.2
F14	DDR4_2_DQ50	IO_L18N_T2U_N11_AD2N_70	IO_L18N_T2U_N11_AD2N_72	1.2
E13	DDR4_2_DQ51	IO_L15N_T2L_N5_AD11N_70	IO_L15N_T2L_N5_AD11N_72	1.2
E15	DDR4_2_DQ52	IO_L17N_T2U_N9_AD10N_70	IO_L17N_T2U_N9_AD10N_72	1.2
H13	DDR4_2_DQ53	IO_L14N_T2L_N3_GC_70	IO_L14N_T2L_N3_GC_72	1.2
E16	DDR4_2_DQ54	IO_L17P_T2U_N8_AD10P_70	IO_L17P_T2U_N8_AD10P_72	1.2
F13	DDR4_2_DQ55	IO_L15P_T2L_N4_AD11P_70	IO_L15P_T2L_N4_AD11P_72	1.2
J15	DDR4_2_DQ56	IO_L9N_T1L_N5_AD12N_70	IO_L9N_T1L_N5_AD12N_72	1.2
K16	DDR4_2_DQ57	IO_L9P_T1L_N4_AD12P_70	IO_L9P_T1L_N4_AD12P_72	1.2
G15	DDR4_2_DQ58	IO_L11N_T1U_N9_GC_70	IO_L11N_T1U_N9_GC_72	1.2
G16	DDR4_2_DQ59	IO_L11P_T1U_N8_GC_70	IO_L11P_T1U_N8_GC_72	1.2
P24	DDR4_2_DQ6	IO_L5P_T0U_N8_AD14P_72	IO_L5P_T0U_N8_AD14P_74	1.2
J14	DDR4_2_DQ60	IO_L12P_T1U_N10_GC_70	IO_L12P_T1U_N10_GC_72	1.2
M13	DDR4_2_DQ61	IO_L8N_T1L_N3_AD5N_70	IO_L8N_T1L_N3_AD5N_72	1.2
J13	DDR4_2_DQ62	IO_L12N_T1U_N11_GC_70	IO_L12N_T1U_N11_GC_72	1.2
M14	DDR4_2_DQ63	IO_L8P_T1L_N2_AD5P_70	IO_L8P_T1L_N2_AD5P_72	1.2
N13	DDR4_2_DQ64	IO_L5N_T0U_N9_AD14N_70	IO_L5N_T0U_N9_AD14N_72	1.2
T15	DDR4_2_DQ65	IO_L2P_T0L_N2_70	IO_L2P_T0L_N2_72	1.2
P14	DDR4_2_DQ66	IO_L3P_T0L_N4_AD15P_70	IO_L3P_T0L_N4_AD15P_72	1.2
P13	DDR4_2_DQ67	IO_L3N_T0L_N5_AD15N_70	IO_L3N_T0L_N5_AD15N_72	1.2
N14	DDR4_2_DQ68	IO_L5P_T0U_N8_AD14P_70	IO_L5P_T0U_N8_AD14P_72	1.2
R15	DDR4_2_DQ69	IO_L2N_T0L_N3_70	IO_L2N_T0L_N3_72	1.2
T24	DDR4_2_DQ7	IO_L6P_T0U_N10_AD6P_72	IO_L6P_T0U_N10_AD6P_74	1.2
N16	DDR4_2_DQ70	IO_L6P_T0U_N10_AD6P_70	IO_L6P_T0U_N10_AD6P_72	1.2
M16	DDR4_2_DQ71	IO_L6N_T0U_N11_AD6N_70	IO_L6N_T0U_N11_AD6N_72	1.2
A17	DDR4_2_DQ8	IO_L20N_T3L_N3_AD1N_71	IO_L20N_T3L_N3_AD1N_73	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
B20	DDR4_2_DQ9	IO_L21P_T3L_N4_AD8P_71	IO_L21P_T3L_N4_AD8P_73	1.2
R22	DDR4_2_DQS0_C	IO_L4N_T0U_N7_DBC_AD7N_72	IO_L4N_T0U_N7_DBC_AD7N_74	1.2
T22	DDR4_2_DQS0_T	IO_L4P_T0U_N6_DBC_AD7P_72	IO_L4P_T0U_N6_DBC_AD7P_74	1.2
B17	DDR4_2_DQS1_C	IO_L22N_T3U_N7_DBC_AD0N_71	IO_L22N_T3U_N7_DBC_AD0N_73	1.2
C17	DDR4_2_DQS1_T	IO_L22P_T3U_N6_DBC_AD0P_71	IO_L22P_T3U_N6_DBC_AD0P_73	1.2
F17	DDR4_2_DQS2_C	IO_L16N_T2U_N7_QBC_AD3N_71	IO_L16N_T2U_N7_QBC_AD3N_73	1.2
F18	DDR4_2_DQS2_T	IO_L16P_T2U_N6_QBC_AD3P_71	IO_L16P_T2U_N6_QBC_AD3P_73	1.2
K20	DDR4_2_DQS3_C	IO_L10N_T1U_N7_QBC_AD4N_71	IO_L10N_T1U_N7_QBC_AD4N_73	1.2
L20	DDR4_2_DQS3_T	IO_L10P_T1U_N6_QBC_AD4P_71	IO_L10P_T1U_N6_QBC_AD4P_73	1.2
P18	DDR4_2_DQS4_C	IO_L4N_T0U_N7_DBC_AD7N_71	IO_L4N_T0U_N7_DBC_AD7N_73	1.2
P19	DDR4_2_DQS4_T	IO_L4P_T0U_N6_DBC_AD7P_71	IO_L4P_T0U_N6_DBC_AD7P_73	1.2
C13	DDR4_2_DQS5_C	IO_L22N_T3U_N7_DBC_AD0N_70	IO_L22N_T3U_N7_DBC_AD0N_72	1.2
D13	DDR4_2_DQS5_T	IO_L22P_T3U_N6_DBC_AD0P_70	IO_L22P_T3U_N6_DBC_AD0P_72	1.2
G13	DDR4_2_DQS6_C	IO_L16N_T2U_N7_QBC_AD3N_70	IO_L16N_T2U_N7_QBC_AD3N_72	1.2
G14	DDR4_2_DQS6_T	IO_L16P_T2U_N6_QBC_AD3P_70	IO_L16P_T2U_N6_QBC_AD3P_72	1.2
L13	DDR4_2_DQS7_C	IO_L10N_T1U_N7_QBC_AD4N_70	IO_L10N_T1U_N7_QBC_AD4N_72	1.2
L14	DDR4_2_DQS7_T	IO_L10P_T1U_N6_QBC_AD4P_70	IO_L10P_T1U_N6_QBC_AD4P_72	1.2
P15	DDR4_2_DQS8_C	IO_L4N_T0U_N7_DBC_AD7N_70	IO_L4N_T0U_N7_DBC_AD7N_72	1.2
R16	DDR4_2_DQS8_T	IO_L4P_T0U_N6_DBC_AD7P_70	IO_L4P_T0U_N6_DBC_AD7P_72	1.2
E22	DDR4_2_ODT	IO_L17N_T2U_N9_AD10N_72	IO_L17N_T2U_N9_AD10N_74	1.2
A25	DDR4_2_PAR	IO_L22P_T3U_N6_DBC_AD0P_72	IO_L22P_T3U_N6_DBC_AD0P_74	1.2
M22	DDR4_2_RESET_N	IO_L7P_T1L_N0_QBC_AD13P_72	IO_L7P_T1L_N0_QBC_AD13P_74	1.2
G21	DDR4_2_TEN	IO_L18N_T2U_N11_AD2N_72	IO_L18N_T2U_N11_AD2N_74	1.2
C27	DDR4_3_A0	IO_L21P_T3L_N4_AD8P_48	IO_L21P_T3L_N4_AD8P_71	1.2
A27	DDR4_3_A1	IO_L22P_T3U_N6_DBC_AD0P_48	IO_L22P_T3U_N6_DBC_AD0P_71	1.2
B29	DDR4_3_A10	IO_L19N_T3L_N1_DBC_AD9N_48	IO_L19N_T3L_N1_DBC_AD9N_71	1.2
G26	DDR4_3_A11	IO_L14P_T2L_N2_GC_48	IO_L14P_T2L_N2_GC_71	1.2
C28	DDR4_3_A12	IO_L21N_T3L_N5_AD8N_48	IO_L21N_T3L_N5_AD8N_71	1.2
D26	DDR4_3_A13	IO_L23P_T3U_N8_48	IO_L23P_T3U_N8_71	1.2
F28	DDR4_3_A14	IO_L15P_T2L_N4_AD11P_48	IO_L15P_T2L_N4_AD11P_71	1.2
K27	DDR4_3_A15	IO_L9N_T1L_N5_AD12N_48	IO_L9N_T1L_N5_AD12N_71	1.2
K28	DDR4_3_A16	IO_T1U_N12_48	IO_T1U_N12_71	1.2
B26	DDR4_3_A17	IO_L24P_T3U_N10_48	IO_L24P_T3U_N10_71	1.2
J25	DDR4_3_A2	IO_L10P_T1U_N6_QBC_AD4P_48	IO_L10P_T1U_N6_QBC_AD4P_71	1.2
K25	DDR4_3_A3	IO_L8P_T1L_N2_AD5P_48	IO_L8P_T1L_N2_AD5P_71	1.2
J26	DDR4_3_A4	IO_L10N_T1U_N7_QBC_AD4N_48	IO_L10N_T1U_N7_QBC_AD4N_71	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
E27	DDR4_3_A5	IO_L17N_T2U_N9_AD10N_48	IO_L17N_T2U_N9_AD10N_71	1.2
G27	DDR4_3_A6	IO_L14N_T2L_N3_GC_48	IO_L14N_T2L_N3_GC_71	1.2
E26	DDR4_3_A7	IO_T2U_N12_48	IO_T2U_N12_71	1.2
C26	DDR4_3_A8	IO_L23N_T3U_N9_48	IO_L23N_T3U_N9_71	1.2
H26	DDR4_3_A9	IO_L13P_T2L_N0_GC_QBC_48	IO_L13P_T2L_N0_GC_QBC_71	1.2
K26	DDR4_3_ACT_N	IO_L8N_T1L_N3_AD5N_48	IO_L8N_T1L_N3_AD5N_71	1.2
L27	DDR4_3_ALERT_N	IO_L9P_T1L_N4_AD12P_48	IO_L9P_T1L_N4_AD12P_71	1.2
E28	DDR4_3_BA0	IO_L18P_T2U_N10_AD2P_48	IO_L18P_T2U_N10_AD2P_71	1.2
F27	DDR4_3_BA1	IO_L17P_T2U_N8_AD10P_48	IO_L17P_T2U_N8_AD10P_71	1.2
H27	DDR4_3_BG0	IO_L13N_T2L_N1_GC_QBC_48	IO_L13N_T2L_N1_GC_QBC_71	1.2
D28	DDR4_3_BG1	IO_L18N_T2U_N11_AD2N_48	IO_L18N_T2U_N11_AD2N_71	1.2
G29	DDR4_3_C0	IO_L12N_T1U_N11_GC_48	IO_L12N_T1U_N11_GC_71	1.2
F29	DDR4_3_C1	IO_L15N_T2L_N5_AD11N_48	IO_L15N_T2L_N5_AD11N_71	1.2
A30	DDR4_3_C2	IO_L20N_T3L_N3_AD1N_48	IO_L20N_T3L_N3_AD1N_71	1.2
D30	DDR4_3_CK_C	IO_L16N_T2U_N7_QBC_AD3N_48	IO_L16N_T2U_N7_QBC_AD3N_71	1.2
D29	DDR4_3_CK_T	IO_L16P_T2U_N6_QBC_AD3P_48	IO_L16P_T2U_N6_QBC_AD3P_71	1.2
C29	DDR4_3_CKE	IO_L19P_T3L_N0_DBC_AD9P_48	IO_L19P_T3L_N0_DBC_AD9P_71	1.2
A29	DDR4_3_CS0_N	IO_L20P_T3L_N2_AD1P_48	IO_L20P_T3L_N2_AD1P_71	1.2
R28	DDR4_3_DM0	IO_L1P_T0L_N0_DBC_48	IO_L1P_T0L_N0_DBC_71	1.2
C34	DDR4_3_DM1	IO_L19P_T3L_N0_DBC_AD9P_47	IO_L19P_T3L_N0_DBC_AD9P_70	1.2
F32	DDR4_3_DM2	IO_L13P_T2L_N0_GC_QBC_47	IO_L13P_T2L_N0_GC_QBC_70	1.2
M29	DDR4_3_DM3	IO_L7P_T1L_N0_QBC_AD13P_47	IO_L7P_T1L_N0_QBC_AD13P_70	1.2
T30	DDR4_3_DM4	IO_L1P_T0L_N0_DBC_47	IO_L1P_T0L_N0_DBC_70	1.2
C37	DDR4_3_DM5	IO_L19P_T3L_N0_DBC_AD9P_46	IO_L19P_T3L_N0_DBC_AD9P_69	1.2
G37	DDR4_3_DM6	IO_L13P_T2L_N0_GC_QBC_46	IO_L13P_T2L_N0_GC_QBC_69	1.2
H33	DDR4_3_DM7	IO_L7P_T1L_N0_QBC_AD13P_46	IO_L7P_T1L_N0_QBC_AD13P_69	1.2
M34	DDR4_3_DM8	IO_L1P_T0L_N0_DBC_46	IO_L1P_T0L_N0_DBC_69	1.2
P25	DDR4_3_DQ0	IO_L5N_T0U_N9_AD14N_48	IO_L5N_T0U_N9_AD14N_71	1.2
N27	DDR4_3_DQ1	IO_L2P_T0L_N2_48	IO_L2P_T0L_N2_71	1.2
A32	DDR4_3_DQ10	IO_L24P_T3U_N10_47	IO_L24P_T3U_N10_70	1.2
B35	DDR4_3_DQ11	IO_L20P_T3L_N2_AD1P_47	IO_L20P_T3L_N2_AD1P_70	1.2
B32	DDR4_3_DQ12	IO_L23N_T3U_N9_47	IO_L23N_T3U_N9_70	1.2
C32	DDR4_3_DQ13	IO_L21P_T3L_N4_AD8P_47	IO_L21P_T3L_N4_AD8P_70	1.2
B31	DDR4_3_DQ14	IO_L23P_T3U_N8_47	IO_L23P_T3U_N8_70	1.2
C33	DDR4_3_DQ15	IO_L21N_T3L_N5_AD8N_47	IO_L21N_T3L_N5_AD8N_70	1.2
K30	DDR4_3_DQ16	IO_L15P_T2L_N4_AD11P_47	IO_L15P_T2L_N4_AD11P_70	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
E31	DDR4_3_DQ17	IO_L18P_T2U_N10_AD2P_47	IO_L18P_T2U_N10_AD2P_70	1.2
E33	DDR4_3_DQ18	IO_L14P_T2L_N2_GC_47	IO_L14P_T2L_N2_GC_70	1.2
D33	DDR4_3_DQ19	IO_L14N_T2L_N3_GC_47	IO_L14N_T2L_N3_GC_70	1.2
P26	DDR4_3_DQ2	IO_L3N_T0L_N5_AD15N_48	IO_L3N_T0L_N5_AD15N_71	1.2
K31	DDR4_3_DQ20	IO_L15N_T2L_N5_AD11N_47	IO_L15N_T2L_N5_AD11N_70	1.2
J29	DDR4_3_DQ21	IO_L17P_T2U_N8_AD10P_47	IO_L17P_T2U_N8_AD10P_70	1.2
J30	DDR4_3_DQ22	IO_L17N_T2U_N9_AD10N_47	IO_L17N_T2U_N9_AD10N_70	1.2
D31	DDR4_3_DQ23	IO_L18N_T2U_N11_AD2N_47	IO_L18N_T2U_N11_AD2N_70	1.2
F33	DDR4_3_DQ24	IO_L12P_T1U_N10_GC_47	IO_L12P_T1U_N10_GC_70	1.2
L30	DDR4_3_DQ25	IO_L9N_T1L_N5_AD12N_47	IO_L9N_T1L_N5_AD12N_70	1.2
F34	DDR4_3_DQ26	IO_L12N_T1U_N11_GC_47	IO_L12N_T1U_N11_GC_70	1.2
H32	DDR4_3_DQ27	IO_L8N_T1L_N3_AD5N_47	IO_L8N_T1L_N3_AD5N_70	1.2
G30	DDR4_3_DQ28	IO_L11P_T1U_N8_GC_47	IO_L11P_T1U_N8_GC_70	1.2
L29	DDR4_3_DQ29	IO_L9P_T1L_N4_AD12P_47	IO_L9P_T1L_N4_AD12P_70	1.2
N28	DDR4_3_DQ3	IO_L2N_T0L_N3_48	IO_L2N_T0L_N3_71	1.2
F30	DDR4_3_DQ30	IO_L11N_T1U_N9_GC_47	IO_L11N_T1U_N9_GC_70	1.2
H31	DDR4_3_DQ31	IO_L8P_T1L_N2_AD5P_47	IO_L8P_T1L_N2_AD5P_70	1.2
N29	DDR4_3_DQ32	IO_L6N_T0U_N11_AD6N_47	IO_L6N_T0U_N11_AD6N_70	1.2
N32	DDR4_3_DQ33	IO_L3N_T0L_N5_AD15N_47	IO_L3N_T0L_N5_AD15N_70	1.2
P30	DDR4_3_DQ34	IO_L5N_T0U_N9_AD14N_47	IO_L5N_T0U_N9_AD14N_70	1.2
P31	DDR4_3_DQ35	IO_L3P_T0L_N4_AD15P_47	IO_L3P_T0L_N4_AD15P_70	1.2
P29	DDR4_3_DQ36	IO_L6P_T0U_N10_AD6P_47	IO_L6P_T0U_N10_AD6P_70	1.2
M32	DDR4_3_DQ37	IO_L2P_T0L_N2_47	IO_L2P_T0L_N2_70	1.2
R30	DDR4_3_DQ38	IO_L5P_T0U_N8_AD14P_47	IO_L5P_T0U_N8_AD14P_70	1.2
L32	DDR4_3_DQ39	IO_L2N_T0L_N3_47	IO_L2N_T0L_N3_70	1.2
R25	DDR4_3_DQ4	IO_L5P_T0U_N8_AD14P_48	IO_L5P_T0U_N8_AD14P_71	1.2
C36	DDR4_3_DQ40	IO_L23P_T3U_N8_46	IO_L23P_T3U_N8_69	1.2
C39	DDR4_3_DQ41	IO_L21N_T3L_N5_AD8N_46	IO_L21N_T3L_N5_AD8N_69	1.2
B37	DDR4_3_DQ42	IO_L23N_T3U_N9_46	IO_L23N_T3U_N9_69	1.2
A40	DDR4_3_DQ43	IO_L20N_T3L_N3_AD1N_46	IO_L20N_T3L_N3_AD1N_69	1.2
A38	DDR4_3_DQ44	IO_L24N_T3U_N11_46	IO_L24N_T3U_N11_69	1.2
D39	DDR4_3_DQ45	IO_L21P_T3L_N4_AD8P_46	IO_L21P_T3L_N4_AD8P_69	1.2
A37	DDR4_3_DQ46	IO_L24P_T3U_N10_46	IO_L24P_T3U_N10_69	1.2
B40	DDR4_3_DQ47	IO_L20P_T3L_N2_AD1P_46	IO_L20P_T3L_N2_AD1P_69	1.2
F35	DDR4_3_DQ48	IO_L17P_T2U_N8_AD10P_46	IO_L17P_T2U_N8_AD10P_69	1.2
G38	DDR4_3_DQ49	IO_L15P_T2L_N4_AD11P_46	IO_L15P_T2L_N4_AD11P_69	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
L25	DDR4_3_DQ5	IO_L6N_T0U_N11_AD6N_48	IO_L6N_T0U_N11_AD6N_71	1.2
E36	DDR4_3_DQ50	IO_L14P_T2L_N2_GC_46	IO_L14P_T2L_N2_GC_69	1.2
F38	DDR4_3_DQ51	IO_L15N_T2L_N5_AD11N_46	IO_L15N_T2L_N5_AD11N_69	1.2
E35	DDR4_3_DQ52	IO_L17N_T2U_N9_AD10N_46	IO_L17N_T2U_N9_AD10N_69	1.2
E37	DDR4_3_DQ53	IO_L14N_T2L_N3_GC_46	IO_L14N_T2L_N3_GC_69	1.2
D38	DDR4_3_DQ54	IO_L18N_T2U_N11_AD2N_46	IO_L18N_T2U_N11_AD2N_69	1.2
E38	DDR4_3_DQ55	IO_L18P_T2U_N10_AD2P_46	IO_L18P_T2U_N10_AD2P_69	1.2
H36	DDR4_3_DQ56	IO_L11P_T1U_N8_GC_46	IO_L11P_T1U_N8_GC_69	1.2
J36	DDR4_3_DQ57	IO_L12P_T1U_N10_GC_46	IO_L12P_T1U_N10_GC_69	1.2
G35	DDR4_3_DQ58	IO_L9N_T1L_N5_AD12N_46	IO_L9N_T1L_N5_AD12N_69	1.2
H37	DDR4_3_DQ59	IO_L12N_T1U_N11_GC_46	IO_L12N_T1U_N11_GC_69	1.2
R26	DDR4_3_DQ6	IO_L3P_T0L_N4_AD15P_48	IO_L3P_T0L_N4_AD15P_71	1.2
G36	DDR4_3_DQ60	IO_L11N_T1U_N9_GC_46	IO_L11N_T1U_N9_GC_69	1.2
K38	DDR4_3_DQ61	IO_L8N_T1L_N3_AD5N_46	IO_L8N_T1L_N3_AD5N_69	1.2
G34	DDR4_3_DQ62	IO_L9P_T1L_N4_AD12P_46	IO_L9P_T1L_N4_AD12P_69	1.2
K37	DDR4_3_DQ63	IO_L8P_T1L_N2_AD5P_46	IO_L8P_T1L_N2_AD5P_69	1.2
L33	DDR4_3_DQ64	IO_L5P_T0U_N8_AD14P_46	IO_L5P_T0U_N8_AD14P_69	1.2
K35	DDR4_3_DQ65	IO_L6P_T0U_N10_AD6P_46	IO_L6P_T0U_N10_AD6P_69	1.2
K33	DDR4_3_DQ66	IO_L5N_T0U_N9_AD14N_46	IO_L5N_T0U_N9_AD14N_69	1.2
J35	DDR4_3_DQ67	IO_L6N_T0U_N11_AD6N_46	IO_L6N_T0U_N11_AD6N_69	1.2
N34	DDR4_3_DQ68	IO_L2N_T0L_N3_46	IO_L2N_T0L_N3_69	1.2
J33	DDR4_3_DQ69	IO_L3P_T0L_N4_AD15P_46	IO_L3P_T0L_N4_AD15P_69	1.2
M25	DDR4_3_DQ7	IO_L6P_T0U_N10_AD6P_48	IO_L6P_T0U_N10_AD6P_71	1.2
P34	DDR4_3_DQ70	IO_L2P_T0L_N2_46	IO_L2P_T0L_N2_69	1.2
J34	DDR4_3_DQ71	IO_L3N_T0L_N5_AD15N_46	IO_L3N_T0L_N5_AD15N_69	1.2
A33	DDR4_3_DQ8	IO_L24N_T3U_N11_47	IO_L24N_T3U_N11_70	1.2
B36	DDR4_3_DQ9	IO_L20N_T3L_N3_AD1N_47	IO_L20N_T3L_N3_AD1N_70	1.2
M26	DDR4_3_DQS0_C	IO_L4N_T0U_N7_DBC_AD7N_48	IO_L4N_T0U_N7_DBC_AD7N_71	1.2
N26	DDR4_3_DQS0_T	IO_L4P_T0U_N6_DBC_AD7P_48	IO_L4P_T0U_N6_DBC_AD7P_71	1.2
A35	DDR4_3_DQS1_C	IO_L22N_T3U_N7_DBC_AD0N_47	IO_L22N_T3U_N7_DBC_AD0N_70	1.2
A34	DDR4_3_DQS1_T	IO_L22P_T3U_N6_DBC_AD0P_47	IO_L22P_T3U_N6_DBC_AD0P_70	1.2
D35	DDR4_3_DQS2_C	IO_L16N_T2U_N7_QBC_AD3N_47	IO_L16N_T2U_N7_QBC_AD3N_70	1.2
D34	DDR4_3_DQS2_T	IO_L16P_T2U_N6_QBC_AD3P_47	IO_L16P_T2U_N6_QBC_AD3P_70	1.2
G32	DDR4_3_DQS3_C	IO_L10N_T1U_N7_QBC_AD4N_47	IO_L10N_T1U_N7_QBC_AD4N_70	1.2
G31	DDR4_3_DQS3_T	IO_L10P_T1U_N6_QBC_AD4P_47	IO_L10P_T1U_N6_QBC_AD4P_70	1.2
M31	DDR4_3_DQS4_C	IO_L4N_T0U_N7_DBC_AD7N_47	IO_L4N_T0U_N7_DBC_AD7N_70	1.2

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
N31	DDR4_3_DQS4_T	IO_L4P_T0U_N6_DBC_AD7P_47	IO_L4P_T0U_N6_DBC_AD7P_70	1.2
A39	DDR4_3_DQS5_C	IO_L22N_T3U_N7_DBC_AD0N_46	IO_L22N_T3U_N7_DBC_AD0N_69	1.2
B39	DDR4_3_DQS5_T	IO_L22P_T3U_N6_DBC_AD0P_46	IO_L22P_T3U_N6_DBC_AD0P_69	1.2
E40	DDR4_3_DQS6_C	IO_L16N_T2U_N7_QBC_AD3N_46	IO_L16N_T2U_N7_QBC_AD3N_69	1.2
E39	DDR4_3_DQS6_T	IO_L16P_T2U_N6_QBC_AD3P_46	IO_L16P_T2U_N6_QBC_AD3P_69	1.2
H38	DDR4_3_DQS7_C	IO_L10N_T1U_N7_QBC_AD4N_46	IO_L10N_T1U_N7_QBC_AD4N_69	1.2
J38	DDR4_3_DQS7_T	IO_L10P_T1U_N6_QBC_AD4P_46	IO_L10P_T1U_N6_QBC_AD4P_69	1.2
L36	DDR4_3_DQS8_C	IO_L4N_T0U_N7_DBC_AD7N_46	IO_L4N_T0U_N7_DBC_AD7N_69	1.2
L35	DDR4_3_DQS8_T	IO_L4P_T0U_N6_DBC_AD7P_46	IO_L4P_T0U_N6_DBC_AD7P_69	1.2
L28	DDR4_3_ODT	IO_L7N_T1L_N1_QBC_AD13N_48	IO_L7N_T1L_N1_QBC_AD13N_71	1.2
B27	DDR4_3_PAR	IO_L24N_T3U_N11_48	IO_L24N_T3U_N11_71	1.2
M27	DDR4_3_RESET_N	IO_L7P_T1L_N0_QBC_AD13P_48	IO_L7P_T1L_N0_QBC_AD13P_71	1.2
B30	DDR4_3_TEN	IO_T3U_N12_48	IO_T3U_N12_71	1.2
AD12	DONE_1V8	DONE_0	DONE_0	1.8
AM26	EMCCLK_PIN	IO_L24P_T3U_N10_EMCCLK_65	IO_L24P_T3U_N10_EMCCLK_65	1.2
AV19	FABRIC_CLK_N	IO_L12N_T1U_N11_GC_64	IO_L12N_T1U_N11_GC_64	1.8
AU19	FABRIC_CLK_P	IO_L12P_T1U_N10_GC_64	IO_L12P_T1U_N10_GC_64	1.8
H24	FAN_FAIL_1V2_L	IO_L12P_T1U_N10_GC_72	IO_L12P_T1U_N10_GC_74	1.2
AF35	FIREFLY_CLK_0_PIN_N	MGTREFCLK1N_122	MGTREFCLK1N_122	MGT
AF34	FIREFLY_CLK_0_PIN_P	MGTREFCLK1P_122	MGTREFCLK1P_122	MGT
F10	FIREFLY_CLK_1_PIN_N	MGTREFCLK1N_232	MGTREFCLK1N_232	MGT
F11	FIREFLY_CLK_1_PIN_P	MGTREFCLK1P_232	MGTREFCLK1P_232	MGT
BF17	FIREFLY_INT_1V8_L	IO_T2U_N12_64	IO_T2U_N12_64	1.8
BF20	FIREFLY_RST_1V8_L	IO_L19P_T3L_N0_DBC_AD9P_64	IO_L19P_T3L_N0_DBC_AD9P_64	1.8
BD19	FIREFLY_SCL_1V8	IO_L20P_T3L_N2_AD1P_64	IO_L20P_T3L_N2_AD1P_64	1.8
BF19	FIREFLY_SDA_1V8	IO_L19N_T3L_N1_DBC_AD9N_64	IO_L19N_T3L_N1_DBC_AD9N_64	1.8
L17	FIREFLY0_MODPRS_L	IO_T1U_N12_71	IO_T1U_N12_73	1.8
BD18	FIREFLY0_MODSEL_1V8_L	IO_L20N_T3L_N3_AD1N_64	IO_L20N_T3L_N3_AD1N_64	1.8
AN46	FIREFLY0_RX0_N	MGTYRXN0_122	MGTYRXN0_122	MGT
AN45	FIREFLY0_RX0_P	MGTYRXP0_122	MGTYRXP0_122	MGT
AM44	FIREFLY0_RX1_N	MGTYRXN1_122	MGTYRXN1_122	MGT
AM43	FIREFLY0_RX1_P	MGTYRXP1_122	MGTYRXP1_122	MGT
AL46	FIREFLY0_RX2_N	MGTYRXN2_122	MGTYRXN2_122	MGT
AL45	FIREFLY0_RX2_P	MGTYRXP2_122	MGTYRXP2_122	MGT
AK44	FIREFLY0_RX3_N	MGTYRXN3_122	MGTYRXN3_122	MGT
AK43	FIREFLY0_RX3_P	MGTYRXP3_122	MGTYRXP3_122	MGT

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AN41	FIREFLY0_TX0_N	MGTYTXN0_122	MGTYTXN0_122	MGT
AN40	FIREFLY0_TX0_P	MGTYTXP0_122	MGTYTXP0_122	MGT
AM39	FIREFLY0_TX1_N	MGTYTXN1_122	MGTYTXN1_122	MGT
AM38	FIREFLY0_TX1_P	MGTYTXP1_122	MGTYTXP1_122	MGT
AL41	FIREFLY0_TX2_N	MGTYTXN2_122	MGTYTXN2_122	MGT
AL40	FIREFLY0_TX2_P	MGTYTXP2_122	MGTYTXP2_122	MGT
AK39	FIREFLY0_TX3_N	MGTYTXN3_122	MGTYTXN3_122	MGT
AK38	FIREFLY0_TX3_P	MGTYTXP3_122	MGTYTXP3_122	MGT
K13	FIREFLY1_MODPRS_L	IO_T1U_N12_70	IO_T1U_N12_72	1.8
BE21	FIREFLY1_MODSEL_1V8_L	IO_L21P_T3L_N4_AD8P_64	IO_L21P_T3L_N4_AD8P_64	1.8
AJ46	FIREFLY1_RX0_N	MGTYRXN0_123	MGTYRXN0_123	MGT
AJ45	FIREFLY1_RX0_P	MGTYRXP0_123	MGTYRXP0_123	MGT
AH44	FIREFLY1_RX1_N	MGTYRXN1_123	MGTYRXN1_123	MGT
AH43	FIREFLY1_RX1_P	MGTYRXP1_123	MGTYRXP1_123	MGT
AG46	FIREFLY1_RX2_N	MGTYRXN2_123	MGTYRXN2_123	MGT
AG45	FIREFLY1_RX2_P	MGTYRXP2_123	MGTYRXP2_123	MGT
AF44	FIREFLY1_RX3_N	MGTYRXN3_123	MGTYRXN3_123	MGT
AF43	FIREFLY1_RX3_P	MGTYRXP3_123	MGTYRXP3_123	MGT
AJ41	FIREFLY1_TX0_N	MGTYTXN0_123	MGTYTXN0_123	MGT
AJ40	FIREFLY1_TX0_P	MGTYTXP0_123	MGTYTXP0_123	MGT
AH39	FIREFLY1_TX1_N	MGTYTXN1_123	MGTYTXN1_123	MGT
AH38	FIREFLY1_TX1_P	MGTYTXP1_123	MGTYTXP1_123	MGT
AG41	FIREFLY1_TX2_N	MGTYTXN2_123	MGTYTXN2_123	MGT
AG40	FIREFLY1_TX2_P	MGTYTXP2_123	MGTYTXP2_123	MGT
AF39	FIREFLY1_TX3_N	MGTYTXN3_123	MGTYTXN3_123	MGT
AF38	FIREFLY1_TX3_P	MGTYTXP3_123	MGTYTXP3_123	MGT
D15	FIREFLY2_MODPRS_L	IO_T2U_N12_70	IO_T2U_N12_72	1.8
BE20	FIREFLY2_MODSEL_1V8_L	IO_L21N_T3L_N5_AD8N_64	IO_L21N_T3L_N5_AD8N_64	1.8
J3	FIREFLY2_RX0_N	MGTYRXN0_232	MGTYRXN0_232	MGT
J4	FIREFLY2_RX0_P	MGTYRXP0_232	MGTYRXP0_232	MGT
H1	FIREFLY2_RX1_N	MGTYRXN1_232	MGTYRXN1_232	MGT
H2	FIREFLY2_RX1_P	MGTYRXP1_232	MGTYRXP1_232	MGT
G3	FIREFLY2_RX2_N	MGTYRXN2_232	MGTYRXN2_232	MGT
G4	FIREFLY2_RX2_P	MGTYRXP2_232	MGTYRXP2_232	MGT
F1	FIREFLY2_RX3_N	MGTYRXN3_232	MGTYRXN3_232	MGT
F2	FIREFLY2_RX3_P	MGTYRXP3_232	MGTYRXP3_232	MGT

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
J8	FIREFLY2_TX0_N	MGTYTXN0_232	MGTYTXN0_232	MGT
J9	FIREFLY2_TX0_P	MGTYTXP0_232	MGTYTXP0_232	MGT
H6	FIREFLY2_TX1_N	MGTYTXN1_232	MGTYTXN1_232	MGT
H7	FIREFLY2_TX1_P	MGTYTXP1_232	MGTYTXP1_232	MGT
G8	FIREFLY2_TX2_N	MGTYTXN2_232	MGTYTXN2_232	MGT
G9	FIREFLY2_TX2_P	MGTYTXP2_232	MGTYTXP2_232	MGT
F6	FIREFLY2_TX3_N	MGTYTXN3_232	MGTYTXN3_232	MGT
F7	FIREFLY2_TX3_P	MGTYTXP3_232	MGTYTXP3_232	MGT
D16	FIREFLY3_MODPRS_L	IO_T3U_N12_70	IO_T3U_N12_72	1.8
BE17	FIREFLY3_MODSEL_1V8_L	IO_L22P_T3U_N6_DBC_AD0P_64	IO_L22P_T3U_N6_DBC_AD0P_64	1.8
E3	FIREFLY3_RX0_N	MGTYRXN0_233	MGTYRXN0_233	MGT
E4	FIREFLY3_RX0_P	MGTYRXP0_233	MGTYRXP0_233	MGT
D1	FIREFLY3_RX1_N	MGTYRXN1_233	MGTYRXN1_233	MGT
D2	FIREFLY3_RX1_P	MGTYRXP1_233	MGTYRXP1_233	MGT
C3	FIREFLY3_RX2_N	MGTYRXN2_233	MGTYRXN2_233	MGT
C4	FIREFLY3_RX2_P	MGTYRXP2_233	MGTYRXP2_233	MGT
A4	FIREFLY3_RX3_N	MGTYRXN3_233	MGTYRXN3_233	MGT
A5	FIREFLY3_RX3_P	MGTYRXP3_233	MGTYRXP3_233	MGT
E8	FIREFLY3_TX0_N	MGTYTXN0_233	MGTYTXN0_233	MGT
E9	FIREFLY3_TX0_P	MGTYTXP0_233	MGTYTXP0_233	MGT
D6	FIREFLY3_TX1_N	MGTYTXN1_233	MGTYTXN1_233	MGT
D7	FIREFLY3_TX1_P	MGTYTXP1_233	MGTYTXP1_233	MGT
C8	FIREFLY3_TX2_N	MGTYTXN2_233	MGTYTXN2_233	MGT
C9	FIREFLY3_TX2_P	MGTYTXP2_233	MGTYTXP2_233	MGT
A8	FIREFLY3_TX3_N	MGTYTXN3_233	MGTYTXN3_233	MGT
A9	FIREFLY3_TX3_P	MGTYTXP3_233	MGTYTXP3_233	MGT
AG12	FPGA_FLASH_CE0_L	RDWR_FCS_B_0	RDWR_FCS_B_0	1.8
AH12	FPGA_FLASH_DQ0	D00_MOSI_0	D00_MOSI_0	1.8
AK12	FPGA_FLASH_DQ1	D01_DIN_0	D01_DIN_0	1.8
AE12	FPGA_FLASH_DQ2	D02_0	D02_0	1.8
AJ12	FPGA_FLASH_DQ3	D03_0	D03_0	1.8
AW19	GPIO_0_1V8_N	IO_L11N_T1U_N9_GC_64	IO_L11N_T1U_N9_GC_64	1.8
AW20	GPIO_0_1V8_P	IO_L11P_T1U_N8_GC_64	IO_L11P_T1U_N8_GC_64	1.8
AV21	GPIO_1_1V8_N	IO_L14N_T2L_N3_GC_64	IO_L14N_T2L_N3_GC_64	1.8
AV22	GPIO_1_1V8_P	IO_L14P_T2L_N2_GC_64	IO_L14P_T2L_N2_GC_64	1.8
AT19	GPIO_2_1V8_N	IO_L10N_T1U_N7_QBC_AD4N_64	IO_L10N_T1U_N7_QBC_AD4N_64	1.8

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AT20	GPIO_2_1V8_P	IO_L10P_T1U_N6_QBC_AD4P_64	IO_L10P_T1U_N6_QBC_AD4P_64	1.8
BF18	GPIO_3_1V8_N	IO_L24N_T3U_N11_64	IO_L24N_T3U_N11_64	1.8
BE18	GPIO_3_1V8_P	IO_L24P_T3U_N10_64	IO_L24P_T3U_N10_64	1.8
V12	INIT_B_1V8	INIT_B_0	INIT_B_0	1.8
AW21	ISO_CLK_1V8	IO_L13P_T2L_N0_GC_QBC_64	IO_L13P_T2L_N0_GC_QBC_64	1.8
BA28	MEM_CLK_0_PIN_N	IO_L11N_T1U_N9_GC_40	IO_L11N_T1U_N9_GC_61	1.2
BA27	MEM_CLK_0_PIN_P	IO_L11P_T1U_N8_GC_40	IO_L11P_T1U_N8_GC_61	1.2
AY26	MEM_CLK_1_PIN_N	IO_L11N_T1U_N9_GC_A11_D27_65	IO_L11N_T1U_N9_GC_A11_D27_65	1.2
AY25	MEM_CLK_1_PIN_P	IO_L11P_T1U_N8_GC_A10_D26_65	IO_L11P_T1U_N8_GC_A10_D26_65	1.2
J23	MEM_CLK_2_PIN_N	IO_L11N_T1U_N9_GC_72	IO_L11N_T1U_N9_GC_74	1.2
J24	MEM_CLK_2_PIN_P	IO_L11P_T1U_N8_GC_72	IO_L11P_T1U_N8_GC_74	1.2
H28	MEM_CLK_3_PIN_N	IO_L11N_T1U_N9_GC_48	IO_L11N_T1U_N9_GC_71	1.2
J28	MEM_CLK_3_PIN_P	IO_L11P_T1U_N8_GC_48	IO_L11P_T1U_N8_GC_71	1.2
AT10	PCIE_LCL_REFCLK_PIN_N	MGTREFCLK0N_225	MGTREFCLK0N_225	MGT
AT11	PCIE_LCL_REFCLK_PIN_P	MGTREFCLK0P_225	MGTREFCLK0P_225	MGT
AW8	PCIE_REFCLK_0_PIN_N	MGTREFCLK0N_224	MGTREFCLK0N_224	MGT
AW9	PCIE_REFCLK_0_PIN_P	MGTREFCLK0P_224	MGTREFCLK0P_224	MGT
AM10	PCIE_REFCLK_1_PIN_N	MGTREFCLK0N_226	MGTREFCLK0N_226	MGT
AM11	PCIE_REFCLK_1_PIN_P	MGTREFCLK0P_226	MGTREFCLK0P_226	MGT
AF1	PCIE_RX0_N	MGTYRXN3_227	MGTYRXN3_227	MGT
AF2	PCIE_RX0_P	MGTYRXP3_227	MGTYRXP3_227	MGT
AG3	PCIE_RX1_N	MGTYRXN2_227	MGTYRXN2_227	MGT
AG4	PCIE_RX1_P	MGTYRXP2_227	MGTYRXP2_227	MGT
AT1	PCIE_RX10_N	MGTYRXN1_225	MGTYRXN1_225	MGT
AT2	PCIE_RX10_P	MGTYRXP1_225	MGTYRXP1_225	MGT
AU3	PCIE_RX11_N	MGTYRXN0_225	MGTYRXN0_225	MGT
AU4	PCIE_RX11_P	MGTYRXP0_225	MGTYRXP0_225	MGT
AV1	PCIE_RX12_N	MGTYRXN3_224	MGTYRXN3_224	MGT
AV2	PCIE_RX12_P	MGTYRXP3_224	MGTYRXP3_224	MGT
AW3	PCIE_RX13_N	MGTYRXN2_224	MGTYRXN2_224	MGT
AW4	PCIE_RX13_P	MGTYRXP2_224	MGTYRXP2_224	MGT
BA1	PCIE_RX14_N	MGTYRXN1_224	MGTYRXN1_224	MGT
BA2	PCIE_RX14_P	MGTYRXP1_224	MGTYRXP1_224	MGT
BC1	PCIE_RX15_N	MGTYRXN0_224	MGTYRXN0_224	MGT
BC2	PCIE_RX15_P	MGTYRXP0_224	MGTYRXP0_224	MGT
AH1	PCIE_RX2_N	MGTYRXN1_227	MGTYRXN1_227	MGT

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AH2	PCIE_RX2_P	MGTYRXP1_227	MGTYRXP1_227	MGT
AJ3	PCIE_RX3_N	MGTYRXN0_227	MGTYRXN0_227	MGT
AJ4	PCIE_RX3_P	MGTYRXP0_227	MGTYRXP0_227	MGT
AK1	PCIE_RX4_N	MGTYRXN3_226	MGTYRXN3_226	MGT
AK2	PCIE_RX4_P	MGTYRXP3_226	MGTYRXP3_226	MGT
AL3	PCIE_RX5_N	MGTYRXN2_226	MGTYRXN2_226	MGT
AL4	PCIE_RX5_P	MGTYRXP2_226	MGTYRXP2_226	MGT
AM1	PCIE_RX6_N	MGTYRXN1_226	MGTYRXN1_226	MGT
AM2	PCIE_RX6_P	MGTYRXP1_226	MGTYRXP1_226	MGT
AN3	PCIE_RX7_N	MGTYRXN0_226	MGTYRXN0_226	MGT
AN4	PCIE_RX7_P	MGTYRXP0_226	MGTYRXP0_226	MGT
AP1	PCIE_RX8_N	MGTYRXN3_225	MGTYRXN3_225	MGT
AP2	PCIE_RX8_P	MGTYRXP3_225	MGTYRXP3_225	MGT
AR3	PCIE_RX9_N	MGTYRXN2_225	MGTYRXN2_225	MGT
AR4	PCIE_RX9_P	MGTYRXP2_225	MGTYRXP2_225	MGT
AF6	PCIE_TX0_PIN_N	MGTYTXN3_227	MGTYTXN3_227	MGT
AF7	PCIE_TX0_PIN_P	MGTYTXP3_227	MGTYTXP3_227	MGT
AG8	PCIE_TX1_PIN_N	MGTYTXN2_227	MGTYTXN2_227	MGT
AG9	PCIE_TX1_PIN_P	MGTYTXP2_227	MGTYTXP2_227	MGT
AT6	PCIE_TX10_PIN_N	MGTYTXN1_225	MGTYTXN1_225	MGT
AT7	PCIE_TX10_PIN_P	MGTYTXP1_225	MGTYTXP1_225	MGT
AU8	PCIE_TX11_PIN_N	MGTYTXN0_225	MGTYTXN0_225	MGT
AU9	PCIE_TX11_PIN_P	MGTYTXP0_225	MGTYTXP0_225	MGT
AV6	PCIE_TX12_PIN_N	MGTYTXN3_224	MGTYTXN3_224	MGT
AV7	PCIE_TX12_PIN_P	MGTYTXP3_224	MGTYTXP3_224	MGT
BB4	PCIE_TX13_PIN_N	MGTYTXN2_224	MGTYTXN2_224	MGT
BB5	PCIE_TX13_PIN_P	MGTYTXP2_224	MGTYTXP2_224	MGT
BD4	PCIE_TX14_PIN_N	MGTYTXN1_224	MGTYTXN1_224	MGT
BD5	PCIE_TX14_PIN_P	MGTYTXP1_224	MGTYTXP1_224	MGT
BF4	PCIE_TX15_PIN_N	MGTYTXN0_224	MGTYTXN0_224	MGT
BF5	PCIE_TX15_PIN_P	MGTYTXP0_224	MGTYTXP0_224	MGT
AH6	PCIE_TX2_PIN_N	MGTYTXN1_227	MGTYTXN1_227	MGT
AH7	PCIE_TX2_PIN_P	MGTYTXP1_227	MGTYTXP1_227	MGT
AJ8	PCIE_TX3_PIN_N	MGTYTXN0_227	MGTYTXN0_227	MGT
AJ9	PCIE_TX3_PIN_P	MGTYTXP0_227	MGTYTXP0_227	MGT
AK6	PCIE_TX4_PIN_N	MGTYTXN3_226	MGTYTXN3_226	MGT

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AK7	PCIE_TX4_PIN_P	MGTYTXP3_226	MGTYTXP3_226	MGT
AL8	PCIE_TX5_PIN_N	MGTYTXN2_226	MGTYTXN2_226	MGT
AL9	PCIE_TX5_PIN_P	MGTYTXP2_226	MGTYTXP2_226	MGT
AM6	PCIE_TX6_PIN_N	MGTYTXN1_226	MGTYTXN1_226	MGT
AM7	PCIE_TX6_PIN_P	MGTYTXP1_226	MGTYTXP1_226	MGT
AN8	PCIE_TX7_PIN_N	MGTYTXN0_226	MGTYTXN0_226	MGT
AN9	PCIE_TX7_PIN_P	MGTYTXP0_226	MGTYTXP0_226	MGT
AP6	PCIE_TX8_PIN_N	MGTYTXN3_225	MGTYTXN3_225	MGT
AP7	PCIE_TX8_PIN_P	MGTYTXP3_225	MGTYTXP3_225	MGT
AR8	PCIE_TX9_PIN_N	MGTYTXN2_225	MGTYTXN2_225	MGT
AR9	PCIE_TX9_PIN_P	MGTYTXP2_225	MGTYTXP2_225	MGT
AY21	PERST_1V8_L	IO_L13N_T2L_N1_GC_QBC_64	IO_L13N_T2L_N1_GC_QBC_64	1.8
AP26	PERSTN0	IO_T3U_N12_PERSTN0_65	IO_T3U_N12_PERSTN0_65	1.8
D36	QSFP_INT_1V2_L	IO_T2U_N12_46	IO_T2U_N12_69	1.2
BD20	QSFP_LPMODE_1V8	IO_L23N_T3U_N9_64	IO_L23N_T3U_N9_64	1.8
D40	QSFP_MODPRS_1V2_L	IO_T3U_N12_46	IO_T3U_N12_69	1.2
BB20	QSFP_RST_1V8_L	IO_T3U_N12_64	IO_T3U_N12_64	1.8
U3	QSFP_RX0_N	MGTYRXN0_230	MGTYRXN0_230	MGT
U4	QSFP_RX0_P	MGTYRXP0_230	MGTYRXP0_230	MGT
T1	QSFP_RX1_N	MGTYRXN1_230	MGTYRXN1_230	MGT
T2	QSFP_RX1_P	MGTYRXP1_230	MGTYRXP1_230	MGT
R3	QSFP_RX2_N	MGTYRXN2_230	MGTYRXN2_230	MGT
R4	QSFP_RX2_P	MGTYRXP2_230	MGTYRXP2_230	MGT
P1	QSFP_RX3_N	MGTYRXN3_230	MGTYRXN3_230	MGT
P2	QSFP_RX3_P	MGTYRXP3_230	MGTYRXP3_230	MGT
N3	QSFP_RX4_N	MGTYRXN0_231	MGTYRXN0_231	MGT
N4	QSFP_RX4_P	MGTYRXP0_231	MGTYRXP0_231	MGT
M1	QSFP_RX5_N	MGTYRXN1_231	MGTYRXN1_231	MGT
M2	QSFP_RX5_P	MGTYRXP1_231	MGTYRXP1_231	MGT
L3	QSFP_RX6_N	MGTYRXN2_231	MGTYRXN2_231	MGT
L4	QSFP_RX6_P	MGTYRXP2_231	MGTYRXP2_231	MGT
K1	QSFP_RX7_N	MGTYRXN3_231	MGTYRXN3_231	MGT
K2	QSFP_RX7_P	MGTYRXP3_231	MGTYRXP3_231	MGT
BE16	QSFP_SCL_1V8	IO_L22N_T3U_N7_DBC_AD0N_64	IO_L22N_T3U_N7_DBC_AD0N_64	1.8
BD21	QSFP_SDA_1V8	IO_L23P_T3U_N8_64	IO_L23P_T3U_N8_64	1.8
U8	QSFP_TX0_N	MGTYTXN0_230	MGTYTXN0_230	MGT

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
U9	QSFP_TX0_P	MGTYTXP0_230	MGTYTXP0_230	MGT
T6	QSFP_TX1_N	MGTYTXN1_230	MGTYTXN1_230	MGT
T7	QSFP_TX1_P	MGTYTXP1_230	MGTYTXP1_230	MGT
R8	QSFP_TX2_N	MGTYTXN2_230	MGTYTXN2_230	MGT
R9	QSFP_TX2_P	MGTYTXP2_230	MGTYTXP2_230	MGT
P6	QSFP_TX3_N	MGTYTXN3_230	MGTYTXN3_230	MGT
P7	QSFP_TX3_P	MGTYTXP3_230	MGTYTXP3_230	MGT
N8	QSFP_TX4_N	MGTYTXN0_231	MGTYTXN0_231	MGT
N9	QSFP_TX4_P	MGTYTXP0_231	MGTYTXP0_231	MGT
M6	QSFP_TX5_N	MGTYTXN1_231	MGTYTXN1_231	MGT
M7	QSFP_TX5_P	MGTYTXP1_231	MGTYTXP1_231	MGT
L8	QSFP_TX6_N	MGTYTXN2_231	MGTYTXN2_231	MGT
L9	QSFP_TX6_P	MGTYTXP2_231	MGTYTXP2_231	MGT
K6	QSFP_TX7_N	MGTYTXN3_231	MGTYTXN3_231	MGT
K7	QSFP_TX7_P	MGTYTXP3_231	MGTYTXP3_231	MGT
P10	QSFP-DD_CLK_PIN_N	MGTREFCLK1N_230	MGTREFCLK1N_230	MGT
P11	QSFP-DD_CLK_PIN_P	MGTREFCLK1P_230	MGTREFCLK1P_230	MGT
AL21	SI5328_0_1V8_INT_C1B	IO_L2P_T0L_N2_64	IO_L2P_T0L_N2_64	1.8
AP21	SI5328_0_1V8_LOL	IO_L3P_T0L_N4_AD15P_64	IO_L3P_T0L_N4_AD15P_64	1.8
AL20	SI5328_0_1V8_RST_L	IO_L2N_T0L_N3_64	IO_L2N_T0L_N3_64	1.8
K10	SI5328_0_IN_0_N	MGTREFCLK1N_231	MGTREFCLK1N_231	MGT
K11	SI5328_0_IN_0_P	MGTREFCLK1P_231	MGTREFCLK1P_231	MGT
AU22	SI5328_0_IN_1_N	IO_L9N_T1L_N5_AD12N_64	IO_L9N_T1L_N5_AD12N_64	1.8
AT22	SI5328_0_IN_1_P	IO_L9P_T1L_N4_AD12P_64	IO_L9P_T1L_N4_AD12P_64	1.8
T10	SI5328_0_OUT_0_PIN_N	MGTREFCLK0N_230	MGTREFCLK0N_230	MGT
T11	SI5328_0_OUT_0_PIN_P	MGTREFCLK0P_230	MGTREFCLK0P_230	MGT
M10	SI5328_0_OUT_1_PIN_N	MGTREFCLK0N_231	MGTREFCLK0N_231	MGT
M11	SI5328_0_OUT_1_PIN_P	MGTREFCLK0P_231	MGTREFCLK0P_231	MGT
AP20	SI5328_1_1V8_INT_C1B	IO_L3N_T0L_N5_AD15N_64	IO_L3N_T0L_N5_AD15N_64	1.8
AM19	SI5328_1_1V8_LOL	IO_L4N_T0U_N7_DBC_AD7N_64	IO_L4N_T0U_N7_DBC_AD7N_64	1.8
AL19	SI5328_1_1V8_RST_L	IO_L4P_T0U_N6_DBC_AD7P_64	IO_L4P_T0U_N6_DBC_AD7P_64	1.8
AD35	SI5328_1_IN_0_N	MGTREFCLK1N_123	MGTREFCLK1N_123	MGT
AD34	SI5328_1_IN_0_P	MGTREFCLK1P_123	MGTREFCLK1P_123	MGT
BC18	SI5328_1_IN_1_N	IO_L15N_T2L_N5_AD11N_64	IO_L15N_T2L_N5_AD11N_64	1.8
BC19	SI5328_1_IN_1_P	IO_L15P_T2L_N4_AD11P_64	IO_L15P_T2L_N4_AD11P_64	1.8
AG37	SI5328_1_OUT_0_PIN_N	MGTREFCLK0N_122	MGTREFCLK0N_122	MGT

Table 13 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name (VU9P)	Pin Name (VU13P)	Bank Voltage
AG36	SI5328_1_OUT_0_PIN_P	MGTREFCLK0P_122	MGTREFCLK0P_122	MGT
AE37	SI5328_1_OUT_1_PIN_N	MGTREFCLK0N_123	MGTREFCLK0N_123	MGT
AE36	SI5328_1_OUT_1_PIN_P	MGTREFCLK0P_123	MGTREFCLK0P_123	MGT
AP19	SI5328_1V8_SCL	IO_L1N_T0L_N1_DBC_64	IO_L1N_T0L_N1_DBC_64	1.8
AN19	SI5328_1V8_SDA	IO_L1P_T0L_N0_DBC_64	IO_L1P_T0L_N0_DBC_64	1.8
AN22	SI5328_2_1V8_INT_C1B	IO_L5P_T0U_N8_AD14P_64	IO_L5P_T0U_N8_AD14P_64	1.8
AM21	SI5328_2_1V8_LOL	IO_L6P_T0U_N10_AD6P_64	IO_L6P_T0U_N10_AD6P_64	1.8
AN21	SI5328_2_1V8_RST_L	IO_L5N_T0U_N9_AD14N_64	IO_L5N_T0U_N9_AD14N_64	1.8
B10	SI5328_2_IN_0_N	MGTREFCLK1N_233	MGTREFCLK1N_233	MGT
B11	SI5328_2_IN_0_P	MGTREFCLK1P_233	MGTREFCLK1P_233	MGT
BA20	SI5328_2_IN_1_N	IO_L16N_T2U_N7_QBC_AD3N_64	IO_L16N_T2U_N7_QBC_AD3N_64	1.8
AY20	SI5328_2_IN_1_P	IO_L16P_T2U_N6_QBC_AD3P_64	IO_L16P_T2U_N6_QBC_AD3P_64	1.8
H10	SI5328_2_OUT_0_PIN_N	MGTREFCLK0N_232	MGTREFCLK0N_232	MGT
H11	SI5328_2_OUT_0_PIN_P	MGTREFCLK0P_232	MGTREFCLK0P_232	MGT
D10	SI5328_2_OUT_1_PIN_N	MGTREFCLK0N_233	MGTREFCLK0N_233	MGT
D11	SI5328_2_OUT_1_PIN_P	MGTREFCLK0P_233	MGTREFCLK0P_233	MGT
AM20	SPARE_SCL	IO_L6N_T0U_N11_AD6N_64	IO_L6N_T0U_N11_AD6N_64	1.8
AR20	SPARE_SDA	IO_T0U_N12_VRP_64	IO_T0U_N12_VRP_64	1.8
AU21	SPARE_WP	IO_L7P_T1L_N0_QBC_AD13P_64	IO_L7P_T1L_N0_QBC_AD13P_64	1.8
BC21	SRVC_MD_1V8_L	IO_L17N_T2U_N9_AD10N_64	IO_L17N_T2U_N9_AD10N_64	1.8
AU20	USER_LED_0_1V8	IO_L7N_T1L_N1_QBC_AD13N_64	IO_L7N_T1L_N1_QBC_AD13N_64	1.8
AR22	USER_LED_1_1V8	IO_L8P_T1L_N2_AD5P_64	IO_L8P_T1L_N2_AD5P_64	1.8
AR21	USER_LED_2_1V8	IO_L8N_T1L_N3_AD5N_64	IO_L8N_T1L_N3_AD5N_64	1.8
AM22	USER_LED_3_1V8	IO_T1U_N12_64	IO_T1U_N12_64	1.8
D21	USR_SW_0	IO_T2U_N12_71	IO_T2U_N12_73	1.8
D18	USR_SW_1	IO_T3U_N12_71	IO_T3U_N12_73	1.8

Table 13 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
6 July 2021	1.0	K. Roth	Initial release.
8 July 2021	1.1	K. Roth	Extensive edits throughout.
3 Dec 2021	1.2	K. Roth	Added thermal performance information to Thermal Performance, 2-slot details to Physical Specifications, and FireFly opening image to FireFly
8 Mar 2022	1.3	K. Roth	Updated product photo to match final heat sink selection ADM-PCIE-9V7 1-slot Product Photo, Added FireFly example part numbers to FireFly
31 May 2022	1.4	K. Roth	Added details about standalone operation in Power Requirements, added details about mechanical retention in Mechanical Requirements
10 Oct 2022	1.5	K. Roth	Removed reference to PCIe gen4 in Key Features
17 Jul 2023	1.6	K. Roth	Separated PCB dimensions in Physical Specifications for consistency with other user guides.

Address: Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 10822 West Toller Drive, Suite 250 Littleton, CO 80127
Telephone: (303) 954 8768
Fax: (866) 820 9956 - toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com